L Number	Hits	Search Text	DB	Time stamp
1	827	buffer near5 nitride with (ga b al gallium indium boron aluminum)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/21 08:43
2	280	(buffer near5 nitride with (ga b al gallium indium boron aluminum)) and (metal$4 near5 nitride)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/21 08:44
3	232	((buffer near5 nitride with (ga b al gallium indium boron aluminum)) and (metal$4 near5 nitride)) and mocvd	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/21 08:44
4	209	(((buffer near5 nitride with (ga b al gallium indium boron aluminum)) and (metal$4 near5 nitride)) and mocvd) and (light adj emitting adj diode)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/21 08:49
6	21	((((buffer near5 nitride with (ga b al gallium indium boron aluminum)) and (metal$4 near5 nitride)) and mocvd) and (light adj emitting adj diode)) and @ay<2001	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/21 08:50

Elastic strain relief in nitridated Ga metal buffer layers for epitaxial GaN growth

Yihwan Kim, Noad A. Shapiro, Henning Feick, Robert Armitage,[a] and Eicke R. Weber
Department of Materials Science and Engineering, University of California at Berkeley, and Materials Science Division, Lawrence Berkeley National Laboratory, Berkeley, California 94720

Yi Yang and Franco Cerrina
Department of Electrical and Computer Engineering, University of Wisconsin-Madison, Madison, Wisconsin 53706

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Gallium nitride epitaxial layers were grown on sapphire by molecular-beam epitaxy using nitridated gallium metal films as buffer layers. The mechanical properties of the buffer layers were investigated and correlated with their chemical composition as determined by synchrotron radiation photoelectron spectroscopy. Biaxial tension experiments were performed by bending the substrates in a pressure cell designed for simultaneous photoluminescence measurements. The shift of the excitonic luminescence peak was used to determine the stress induced in the main GaN epilayer. The fraction of stress transferred from substrate to main layer was as low as 27% for samples grown on nitridated metal buffer layers, compared to nearly 100% for samples on conventional low-temperature GaN buffer layers. The efficiency of stress relief increased in proportion to the fraction of metallic Ga in the nitridated metal buffer layers. These findings suggest GaN films containing residual metallic Ga may serve as compliant buffer layers for heteroepitaxy. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1347016]

Heteroepitaxial growth of GaN on substrates with different lattice constants and thermal expansion coefficients results in significant film stress, leading to high densities of threading dislocations in the epilayer. It is known that the crystal quality of GaN epilayers can be improved by introducing a buffer layer between the epilayer and the substrate.[1,2] Buffer layer growth conditions such as film thickness,[2–4] substrate temperature,[3,5] and N/Ga flux ratio[6–8] were found to significantly affect the material properties and the residual stress of the GaN epilayer. The crystallinity of the GaN epilayer is critically influenced by conditions in the initial growth stage. One of the most important sources of threading defects is the island coalescence boundary. The density of these boundaries is inversely proportional to the adatom surface mobility. The surface mobility of adatoms was found to be strain dependent; compressive strain decreases (and tensile strain increases) the energy barrier for surface diffusion.[9–11] Recently, tensile stress was observed during GaN epilayer growth by *in situ* wafer curvature measurements.[12] Relief of this tensile stress should increase the lateral growth rate and thus improve the crystal quality of the GaN epilayer. In a previous study,[8] we found that a higher Ga/N composition ratio of low temperature GaN (LT GaN) buffer layers improved the material properties of the main GaN epilayers. In order to maximize the benefits of this approach, we adopted a Ga metal film as a buffer layer. Evaporated as a metal, this film is converted into a (nonstoichiometric) GaN template while heating to the epilayer growth temperature in nitrogen plasma ambient. This approach yielded increased electron Hall mobility and reduced x-ray rocking curve widths for our molecular beam epitaxy (MBE)-grown GaN epilayers.[13]

In this letter, we report direct evidence that excess Ga in the buffer layer facilitates stress relief between the sapphire substrate and the GaN epilayer. The sample (GaN main layer/buffer layer/sapphire) was bent *ex situ* with a pressure cell, which applies an additional biaxial tensile strain to the sample. Stress in the GaN main layer is determined from the position of the room-temperature band-edge photoluminescence peak. The variation of the stress in the epilayer with applied pressure was found to depend on the excess Ga content in the buffer layer.

GaN epilayers were grown on *c*-plane sapphire using a Riber 1000 MBE system with a constricted glow discharge nitrogen plasma source.[14] For the growth of GaN epilayers, our unique Ga metal buffer layers as well as conventional LT GaN buffer layers were used. Gallium metal layers were deposited on nitridated sapphire at 500 °C with deposition times ranging from 1 to 10 min. The Ga metal layers were heated up to the main epilayer growth temperature (725 °C) with the nitrogen plasma source on. During this step, the metal layers are partially converted to GaN, and thus referred to as nitridated Ga metal layers. Since the exposure time to the nitrogen plasma was kept constant, the amount of unreacted Ga remaining in the buffer layer is expected to depend solely on the initial Ga film thickness. After buffer layer deposition and annealing, Si-doped GaN main epilayers were grown at 725 °C for 5 min. To investigate the buffer layer properties separately, several buffer layers (of both types) were prepared without the main layer growth step.

The buffer layer thickness was measured by Rutherford backscattering spectroscopy (RBS). X-ray diffraction was

[a]Electronic mail: RDArmitage@lbl.gov

employed to assess the crystallinity of the nitridated Ga metal layers. To verify the presence of metallic Ga in the buffer layers, a synchrotron radiation photoelectron spectroscopy study was carried out on the MAXIMUM photoemission microscope at the undulator Beamline 12 of the Advanced Light Source at Lawrence Berkeley National Laboratory.[15] A monochromatic beam with photon energy of 130 eV was focused on the sample surface with spot size 0.75 μm.

The design of the biaxial pressure cell and the mathematics used to calculate the photoluminescence peak position as a function of the cell pressure have been described elsewhere.[16] The sample serves as a circular window of the cell with the sapphire side facing a pressure-transmitting fluid (mineral oil). When the cell is pressurized, the sample is bent outward and biaxial tensile stress results. The radius of the circular window was 3.175 mm, and the sample thickness (substrate and epilayer) was measured by optical microscopy. Pressure was applied up to 900 psi, which corresponds to an in-plane strain of 5.1×10^{-4} in the 440 μm thick sapphire substrate.

The geometry of the pressure cell allows for simultaneous room-temperature photoluminescence measurements. Spectra were recorded using a 325 nm He–Cd laser as excitation source and a 0.85 m double monochromator equipped with a GaAs photomultiplier for luminescence light dispersion and detection, respectively. A shift of the band-to-band transition in the GaN epilayer was observed as a function of applied pressure.

The thickness of the nitridated Ga metal layers ranged from 3.8 to 24 nm, depending on the initial Ga metal deposition time. The LT GaN buffer layer used for growing a reference GaN epilayer was 50 nm thick. X-ray diffraction revealed that heating of Ga metal layers to the main epilayer growth temperature under nitrogen plasma produces highly oriented GaN crystals.[14] Figure 1(a) shows the photoemission spectra of a nitridated Ga metal layer. Two peaks, related to the Ga3d core level, are clearly resolved. The peak at lower kinetic energy corresponds to Ga3d from GaN, and the higher kinetic energy peak corresponds to Ga3d from metallic Ga.[17] Evidently, some Ga remains in metallic form in the nitridated Ga metal layers. Figure 1(b) shows, as a function of Ga metal layer thickness, the change of the peak-area ratio of Ga3d from the metal to the Ga3d from GaN. As the Ga metal layer thickness increases, the Ga metal fraction increases in the nitridated Ga metal layer. This result is expected, since all Ga metal layers were exposed to nitrogen plasma for the same time. The LT GaN buffer layer was confirmed to contain no metallic Ga.

Figure 2 shows the observed redshift of the band-to-band transition for a GaN main layer on a nitridated Ga metal buffer layer (Ga deposition time=10 min) and for a GaN layer grown on a standard LT GaN buffer layer. The dashed line represents the calculated shift of the band-gap energy of GaN assuming the same strain in the sapphire substrate and the GaN epilayer. While the sample with the LT GaN layer shows an experimental redshift in good agreement with theory, the redshift for the sample with the nitridated Ga metal layer was only 27% of the calculated value. This demonstrates that the nitridated Ga metal buffer layer relieves strain. This stress relief is elastic because no distinct hysteresis of the band-gap energy variation was observed in pressure cycling. The same experiment was carried out for samples with different Ga metal layer thickness, and Fig. 3 clearly shows different degrees of strain transfer from the bent sapphire to the GaN epilayers. The elastic strain relief is more effective for nitridated metal layers containing higher fractions of unreacted Ga. The presence of a "soft" Ga

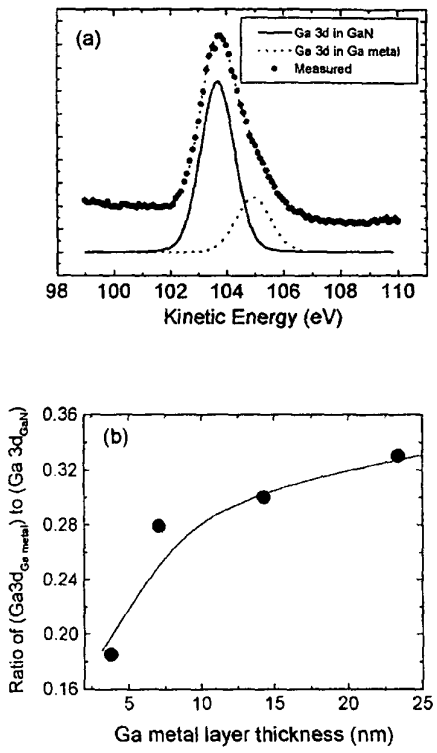

FIG. 1. (a) Photoemission spectrum of Ga 3d core level from the nitridated Ga metal layer deposited for 10 min. Two components from metallic Ga and from GaN are clearly resolved. (b) The ratio of Ga 3d from metallic Ga to Ga 3d from GaN as a function of the Ga metal buffer layer thickness. The ratio was determined from the peak areas of the Ga 3d core levels.

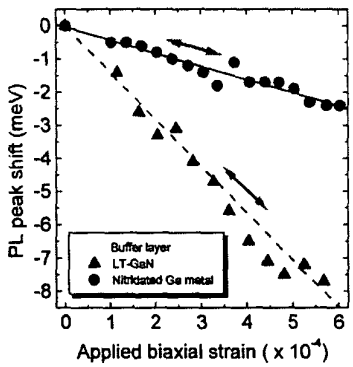

FIG. 2. Redshift of the PL peak position of a GaN layer grown on a Ga metal buffer layer deposited for 10 min (solid circle symbols) and a GaN layer grown on a LT GaN buffer layer (solid triangle symbols) as a function of applied biaxial strain in the sapphire. The dashed line represents the calculated shift of the GaN band gap assuming the same strain in the sapphire substrate and the GaN epilayer. The solid line is a linear fit to the results from the sample with the Ga metal layer. Arrows represent pressure cycling.

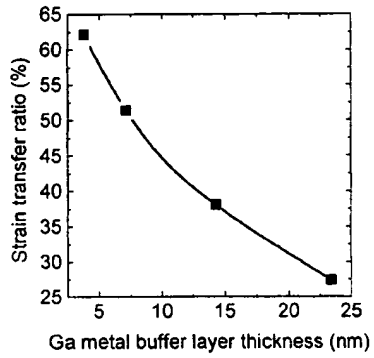

FIG. 3. The ratio of strain transfer (the ratio of the measured redshift to the calculated value) from the strained sapphire to the GaN epilayers as a function of Ga metal buffer layer thickness. Note that an increase of Ga metal layer thickness results in higher metallic Ga content in the nitridated Ga metal buffer layer.

metal component (melting point 30 °C) in the buffer layer significantly increases its compliance to relieve strain even at room temperature. One would expect an even greater degree of stress relief at the GaN growth temperature (725 °C). Thus, a nitridated Ga metal layer provides an effective stress buffer for the subsequent epilayer growth. Therefore, less dislocation generation is necessary for stress relief in the main epilayer, in agreement with the improved material properties of GaN epilayers grown on nitridated Ga metal films.[14] Similar conclusions have been drawn by Kachi *et al.*[18] who utilized an InN buffer layer.

In conclusion, our pressure experiments directly demonstrated the efficient stress relief of heteroepitaxial GaN layers grown with nitridated Ga metal buffer layers. Nitridated Ga metal buffer layers were found to contain Ga metal using synchrotron radiation photoelectron spectroscopy. Even at room temperature this buffer layer elastically reduces the stress generated by the sapphire substrate bent in the pressure cell. The degree of stress relief increases with the Ga metal fraction in the buffer layer, whereas stoichiometric LT GaN buffer layers (without Ga metal) transfer almost 100% of the applied stress to the GaN epilayer. The increased compliance observed is attributed to the presence of Ga metal in the buffer layer.

This work was supported by the Director, Office of Science, Basic Energy Sciences, Division of Materials Sciences, of the U.S. Department of Energy under Contract No. DE-AC03-76SF00098. The authors are grateful to K. M. Yu for the RBS analysis. MAXIMUM is supported by the U.S. Department of Energy under Contract No. DE-FG02-96ER45569.

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L44 ANSWER 1 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2003:118150 HCAPLUS
DN 138:162114
TI Design of semiconductor structures and devices not lattice matched to the substrate
IN Eisenbeiser, Kurt; Ramdani, Jamal
PA Motorola, Inc., USA
SO PCT Int. Appl., 67 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
WO 2003012841	A2	20030213	WO 2002-US15844	20020516

PI WO 2003012841 A2 20030213 WO 2002-US15844 20020516
W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG
PRAI US 2001-911490 A 20010725
AB The invention relates to semiconductor structures and devices not lattice matched to the substrate. High quality epitaxial layers of monocryst. materials are grown overlying monocryst. substrates, such as large silicon wafers, by forming a compliant substrate for growing the monocryst. layers. An accommodating **buffer layer** consists of a layer of monocryst. oxide spaced apart from the silicon wafer by an amorphous interface layer of silicon oxide. The amorphous interface layer dissipates strain and permits the growth of a high quality monocryst. oxide-accommodating **buffer layer**. The accommodating **buffer layer** is substantially lattice matched to both the underlying silicon wafer and the overlying monocryst. material layer. Any lattice mismatch between the accommodating **buffer layer** and the underlying silicon substrate is taken care of by the amorphous interface layer. In addn., formation of a compliant substrate may include utilizing surfactant-enhanced epitaxy, **epitaxial growth** of single crystal silicon onto single crystal oxide, and **epitaxial growth** of Zintl phase materials.

L44 ANSWER 2 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2003:77237 HCAPLUS
DN 138:129880
TI Increased efficiency semiconductor devices including intermetallic layer
IN Talin, Albert A.; Demkov, Alexander A.; Holm, Paige M.
PA Motorola, Inc., USA
SO U.S. Pat. Appl. Publ., 53 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2003020104	A1	20030130	US 2001-911484	20010725

PI US 2003020104 A1 20030130 US 2001-911484 20010725
PRAI US 2001-911484 20010725
AB High quality epitaxial layers of monocryst. materials can be grown overlying monocryst. substrates such as large Si wafers by forming a

compliant substrate for growing the monocryst. layers. An accommodating **buffer layer** comprises a layer of monocryst. oxide spaced apart from a Si wafer by an amorphous interface layer of Si oxide. The amorphous interface layer dissipates strain and permits the growth of a high quality monocryst. oxide accommodating **buffer layer**. The accommodating **buffer layer** is lattice matched to both the underlying Si wafer and the overlying monocryst. material layer. Any lattice mismatch between the accommodating **buffer layer** and the underlying Si substrate is taken care of by the amorphous interface layer. Formation of a compliant substrate may include using surfactant enhanced epitaxy, **epitaxial growth** of single crystal Si onto single crystal oxide, and **epitaxial growth** of Zintl phase materials. Dual gate field effect transistors exhibiting increased transconductance are fabricated using planar processing techniques.

IT **10043-11-5**, Boron nitride, uses **24304-00-5**, Aluminum nitride **25617-97-4**, Gallium nitride
RL: DEV (Device component use); USES (Uses)
(increased efficiency semiconductor devices including intermetallic layer)

IT **7429-90-5**, Aluminum, uses
RL: DEV (Device component use); USES (Uses)
(intermetallic layer component; increased efficiency semiconductor devices including intermetallic layer)

L44 ANSWER 3 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2003:77146 HCAPLUS
DN 138:129855
TI Structures and method for fabricating semiconductor structures and devices utilizing the formation of a compliant **gallium nitride** substrate
IN Ramdani, Jamal; Hilt, Lyndee L.
PA Motorola, Inc., USA
SO U.S. Pat. Appl. Publ., 17 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2003019423	A1	20030130	US 2001-911702	20010725
PRAI US 2001-911702		20010725		

AB High quality epitaxial layers of monocryst. materials can be grown overlying monocryst. substrates such as large Si wafers or compd. semiconductor wafers by forming a compliant substrate for growing the monocryst. layers. In particular, a compliant large area GaN substrate can be fabricated for forming semiconductor structures and devices. An accommodating **buffer layer** comprises a layer of monocryst. oxide spaced apart from a Si wafer by an amorphous interface layer of Si oxide. The amorphous interface layer dissipates strain and permits the growth of a high quality monocryst. oxide accommodating **buffer layer**. The accommodating **buffer layer** is lattice matched to both the underlying Si wafer and the overlying monocryst. material layer. Any lattice mismatch between the accommodating **buffer layer** and the underlying Si substrate is taken care of by the amorphous interface layer. Formation of a compliant large area GaN substrate may include using surfactant enhanced epitaxy, **epitaxial growth** of single crystal Si onto single crystal oxide, and **epitaxial growth** of Zintl phase materials and the resulting large area GaN substrate may be formed as a defect free stand alone substrate.

IT **25617-97-4, Gallium nitride**
RL: FMU (Formation, unclassified); PEP (Physical, engineering or chemical process); PYP (Physical process); TEM (Technical or engineered material use); FORM (Formation, nonpreparative); PROC (Process); USES (Uses)
(structures and method for fabricating semiconductor structures and devices utilizing formation of compliant **gallium nitride** substrate)

IT **7440-55-3, Gallium**, processes
RL: PEP (Physical, engineering or chemical process); PYP (Physical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(template layer; structures and method for fabricating semiconductor structures and devices utilizing formation of compliant **gallium nitride** substrate)

L44 ANSWER 4 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2003:4995 HCAPLUS
DN 138:64974
TI Thin film device where ionic crystals are **epitaxially grown** on a Si single crystal substrate through a proper **buffer layer** and its fabrication method
IN Koinuma, Hideomi; Kawasaki, Masashi; Chikyow, Toyohiro; Konishi, Yoshinori; Yonezawa, Yoshiyuki; Zo, Yoo Young
PA National Institute for Materials Science, Japan; Tokyo Institute of Technology; Fuji Electric Corporate Research and Development, Ltd.
SO Eur. Pat. Appl., 31 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1271626	A2	20030102	EP 2002-254578	20020628
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO, MK, CY, AL, TR				
PRAI	JP 2001-200000	A	20010629		
	JP 2002-87198	A	20020326		

AB A ZnS layer is 1st deposited on a Si single crystal substrate. Ionic crystal thin films (an n-GaN layer, a GaN layer, and a p-GaN layer) are deposited thereon. The ZnS thin film is an oriented film excellent in crystallinity and has excellent surface flatness. When ZnS can be once **epitaxially grown** on the Si single crystal substrate, the ionic crystal thin films can be easily **epitaxially grown** subsequently. Therefore, ZnS is formed to be a **buffer layer**, whereby even ionic crystals having differences in lattice consts. from Si can be easily **epitaxially grown** in an epitaxial thin film with few lattice defects on the Si single crystal substrate. The characteristics of a thin film device using it can be enhanced.

IT **7429-90-5**, Aluminum, uses
RL: DEV (Device component use); MOA (Modifier or additive use); USES (Uses)
(**buffer layer**; thin film device where ionic crystals are **epitaxially grown** on Si single crystal substrate through **buffer layer** of Al-doped zinc oxide or sulfide)

IT **25617-97-4**, Gallium nitride (GaN)
RL: DEV (Device component use); FMU (Formation, unclassified); PEP (Physical, engineering or chemical process); PYP (Physical process); FORM (Formation, nonpreparative); PROC (Process); USES (Uses)
(ionic crystals; thin film device where ionic crystals are

epitaxially grown on Si single crystal substrate through proper **buffer layer** and its fabrication method)

L44 ANSWER 5 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:833229 HCAPLUS
DN 137:317723
TI **Buffer layer** of light emitting semiconductor device and method of fabricating the same
IN Chyi, Jen-Inn
PA Taiwan
SO U.S. Pat. Appl. Publ., 6 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002158258	A1	20021031	US 2002-39199	20020104
PRAI TW 2001-90110239	A	20010427		

AB A **buffer layer** of a light emitting semiconductor device comprising a substrate, the **buffer layer** disposed on the substrate, an light emitting semiconductor layer, and electrodes for inputting voltage is described comprising a **metal layer** (e.g., In, Al, B, Ga) formed on the substrate; and a metallic nitride layer, which is formed on the **metal layer** by transforming part of the **metal layer** into metallic nitride layer (e.g., InN, AlN, BN, GaN), wherein the substrate is selected from sapphire, SiC, silicon, GaAs, InP, AlN, GaP, GaN, and ZnSe. A method of prepg. the **buffer layer** of a light emitting semiconductor device is also described entailing providing a substrate; forming a **metal layer** on the substrate by supplying an org. metal gas; and forming a metallic nitride layer by supplying a nitride gas to react with part of the **metal layer**. The method is characterized in that the reaction gas is supplied sep. and the **buffer layer** is formed with 2 steps or multiple steps to reduce the cleaning times and material waste, thereby realizing a cost-down and efficient manufg. process and may also prevent reaction gas crystg. in gas supplying pipes.

IT **7429-90-5**, Aluminum, uses **7440-42-8**, Boron, uses **7440-55-3**, Gallium, uses **7440-74-6**, Indium, uses
RL: DEV (Device component use); USES (Uses)
(**metal layer** for **buffer layer**; **buffer layer** of light emitting semiconductor device and fabrication)

IT **24304-00-5**, Aluminum nitride (AlN) **25617-97-4**, Gallium nitride (GaN)
RL: DEV (Device component use); USES (Uses)
(**metal nitride** layer for **buffer layer**, substrate; **buffer layer** of light emitting semiconductor device and fabrication)

IT **10043-11-5**, Boron nitride (BN), uses **25617-98-5**, Indium nitride (InN)
RL: DEV (Device component use); USES (Uses)
(**metal nitride** layer for **buffer layer**; **buffer layer** of light emitting semiconductor device and fabrication)

L44 ANSWER 6 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:664860 HCAPLUS
DN 138:47734

03/21/2003

TI **Buffer**-facilitated **epitaxial growth** of AlN on Al2O3(0 0 0 1) at room temperature
AU Lin, Yan-Ru; Wu, Shinn-Tyan
CS Department of Materials Science and Engineering, National Tsing-Hua University, Hsinchu, 30043, Taiwan
SO Surface Science (2002), 516(3), L535-L539
CODEN: SUSCAS; ISSN: 0039-6028
PB Elsevier Science B.V.
DT Journal
LA English
AB Aluminum nitride (AlN) was deposited on Al2O3(0 0 0 1) by d.c. magnetron sputtering. It was discovered that the nitride could grow epitaxially near room temp. A FWHM of 2.degree. was obtained from X-ray rocking curve. A thin compliant **buffer** of aluminum (Al) was sandwiched between nitride and sapphire. The **buffer layer** was nitrided before the commencement of AlN deposition. Both electron and X-ray diffraction data are used to support our contention.
IT **24304-00-5**, Aluminum nitride
RL: PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process)
(**buffer**-facilitated **epitaxial growth** of AlN on Al2O3(0 0 0 1) at room temp.)
IT **7429-90-5**, Aluminum, processes
RL: PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process)
(**buffer**; **buffer**-facilitated **epitaxial growth** of AlN on Al2O3(0 0 0 1) at room temp.)
RE.CNT 24 THERE ARE 24 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 7 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:658403 HCAPLUS
DN 137:193941
TI Copper interconnect structure having diffusion barrier with a reactive **metal layer** for integrated circuits
IN Kim, Ki-Bum; Raaijmakers, Ivo; Soininen, Pekka J.
PA Asm Microchemistry Oy, Finland; Asm America, Inc.
SO PCT Int. Appl., 28 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2002067319	A2	20020829	WO 2001-US47592	20011205
	W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
	RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG				
	US 2002187631	A1	20021212	US 2001-7304	20011205
PRAI	KR 2000-74025	A	20001206		

AB The present invention provides a method of fabricating a semiconductor device, which could advance the commercialization of semiconductor devices with a Cu interconnect by using a reactive **metal layer** as part of the diffusion barrier. For example, in a process of metal interconnect line fabrication, a TiN thin film combined with an Al

intermediate layer was used as a diffusion barrier on trench or via walls. For the formation, Al is deposited on the TiN thin film followed by Cu filling the trench. Al diffuses to TiN layer and reacts with O or N, which will stuff grain boundaries efficiently, thereby blocking the diffusion of Cu successfully.

IT **7429-90-5**, Aluminum, processes
RL: CPS (Chemical process); DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(copper interconnect structure having diffusion barrier with reactive **metal layer** for integrated circuits)

IT **24304-00-5P**, Aluminum nitride
RL: DEV (Device component use); PNU (Preparation, unclassified); PREP (Preparation); USES (Uses)
(copper interconnect structure having diffusion barrier with reactive **metal layer** for integrated circuits)

L44 ANSWER 8 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:505142 HCAPLUS
DN 137:71423
TI Structure and method for fabricating III-V nitride devices utilizing the formation of a compliant substrate
IN Hilt, Lyndee L.; Ramdani, Jamal
PA Motorola, Inc., USA
SO U.S. Pat. Appl. Publ., 18 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002084461	A1	20020704	US 2001-753808	20010103
	WO 2002054468	A2	20020711	WO 2001-US46991	20011206
	WO 2002054468	A3	20030227		
	W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
	RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG				
	US 2002149023	A1	20021017	US 2002-161743	20020605
PRAI	US 2001-753808	A	20010103		

AB Semiconductor structures are described which comprise a monocryst. substrate; a **buffer layer** formed on the substrate; an optional monocryst. material layer formed overlying the **buffer layer**; a plurality of patterned features formed of a dielec. material overlying the monocryst. material layer; a seed layer disposed between the plurality of patterned features; and a monocryst. layer formed of III-V nitride material overlying the seed layer and the plurality of patterned features. The **buffer layer** may comprise an oxide selected from the alk. earth **metal** titanates, alk. earth **metal** zirconates, alk. earth **metal** hafnates, alk. earth **metal** tantalates, alk. earth **metal** ruthenates, alk. earth **metal** niobates, and perovskite oxides. An amorphous oxide layer may be provided under the **buffer layer**, and a template layer may be positioned between the **buffer layer** and the first monocryst. material layer. Methods for fabricating the semiconductor structures are described which entail

providing a monocryst. substrate; **epitaxially growing** an accommodating **buffer layer** overlying the substrate; depositing a plurality of patterned features of a dielec. material overlying the accommodating **buffer layer**; forming a seed layer disposed between the plurality of patterned features; and **epitaxially growing** a first monocryst. layer formed of III-V nitride material overlying the seed layer and the plurality of patterned features. The seed layer may be formed by nitridation of a GaAs layer deposited overlying the first monocryst. material layer, carbonization of a Si layer deposited overlying the first monocryst. material layer, or nitridation of the first monocryst. material layer.

IT **25617-97-4**, **Gallium nitride**
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(Group III-V nitride devices and their fabrication with the formation of compliant substrates)

IT **7429-90-5**, **Aluminum**, processes **7440-55-3**, **Gallium**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(template layers contg. monolayers of; Group III-V nitride devices and their fabrication with the formation of compliant substrates)

L44 ANSWER 9 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:450082 HCAPLUS
DN 137:23005
TI Abrasive particles with metallurgically bonded **metal coatings** for abrasive tools
IN Sherman, Andrew J.; Bose, Animesh
PA USA
SO U.S. Pat. Appl. Publ., 7 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002069592	A1	20020613	US 2000-732834	20001207
PRAI US 1999-169549P	P	19991207		

AB The composite particles, particularly useful for cutting tools, grinding wheels and the like, comprise a cubic abrasive core particle (A) and a metallic deposit (B) metallurgically bonded to A, wherein A is selected from diamond, metal carbides, metal borides, **metal nitrides**, and metal oxides, and B is selected from rhenium, ruthenium, osmium and mixts. and alloys thereof. Conventional fabrication procedures such as chem. vapor deposition are employed to form the metallurgical bond forming deposit on the core particles.

IT **7440-42-8D**, Boron, alloys **7440-55-3D**, Gallium, alloys **10043-11-5**, Boron nitride, processes
RL: PEP (Physical, engineering or chemical process); PRP (Properties); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(manuf. of abrasive particles with metallurgically bonded **metal coatings**)

L44 ANSWER 10 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:391818 HCAPLUS
DN 136:403216
TI Color-shifting pigments and films with luminescent coatings
IN Mayer, Thomas; Yamanaka, Stacey A.; Zieba, Jaroslaw
PA Flex Products, Inc., USA
SO PCT Int. Appl., 56 pp.

CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2002040600	A1	20020523	WO 2001-US20916	20010629
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR				
PRAI	US 2000-715934	A	20001117		

AB Interference pigment flakes and films are provided which have luminescent and color-shifting properties. A luminescent material coating structure is provided which partially covers or encapsulates a color-shifting pigment flake, or covers the outer surface of a film. The pigment flakes have a sym. coating structure on opposing sides of a core layer or have an asym. coating structure with all of the layers on one side of the core layer, or are formed with encapsulating coatings around the core layer. The coating structure of the flakes and foils includes a core layer, a dielec. layer overlying the core layer, and an absorber layer overlying the dielec. layer. The luminescent pigment flakes and films exhibit a discrete color shift so as to have a first color at a first angle of incident light or viewing and a second color different from the first color at a second angle of incident light or viewing. The luminescent pigment flakes are dispersible in liq. media such as paints or inks to produce colorant materials for subsequent application to objects or papers. The luminescent films are laminatable on various objects or are formable on a carrier substrate. Typical reflector layers are prepd. from Al, Ag, Cu, Au, Pt, Sn, Ti, Pd, Ni, Co, Rh, Nb, or Cr. Typical dielec. layers are prepd. from metal oxides, metal fluorides, **metal nitrides**, and metal carbides. Typical absorber layers are prepd. from Cr, Ni, Al, Pd, Pt, Ti, V, Co, Fe, Sn, W, Mo, Rh, Nb, C, graphite, Si, Ge, and compds., mixts., or alloys thereof. Typical luminescent materials are fluorescent dye-liq. cryst. polymer combination, cryst. phosphor, and solid or water-sol. quantum dot particles,.

IT **7429-90-5**, Aluminum, uses **7429-90-5D**, Aluminum, compds.
10043-11-5, Boron nitride, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(in luminescent multilayer pigments and films with color-shifting properties)

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 11 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:391817 HCAPLUS
DN 136:403215
TI Luminescent pigments and films with color-shifting properties
IN Coombs, Paul G.; Zieba, Jaroslaw; Bradley, Richard A., Jr.; Lantman, Christopher W.; Mayer, Thomas; Phillips, Roger W.; Yamanaka, Stacey A.
PA Flex Products, Inc., USA
SO PCT Int. Appl., 55 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2002040599	A1	20020523	WO 2001-US20899	20010729
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR				
PRAI	US 2000-715937	A	20001117		

AB The pigment flakes and films have a sym. coating structure on opposing

sides of a core layer or an asym. coating structure with all of the layers on one side of the core layer, or are formed with encapsulating coating around the core layer. The coating structure of the flakes and films includes a core layer, a dielec. layer overlying the core layer, and an absorber layer overlying the dielec. layer. A luminescent material is incorporated into the flakes or films as a sep. layer or as least part of one or more of the other layers. The pigment flakes and films exhibit a discrete color shift so as to have a first color at a first angle of incident light or viewing and a second color different from the first color and a second angle of incident light or viewing. The pigment flakes are dispersible in liq. media such as paints or inks to produce colorant materials for subsequent application to objects or papers. The films are laminatable to various objects or are formable on a carrier substrate. Typical reflector layers are prepd. from Al, Ag, Cu, Au, Pt, Sn, Ti, Pd, Ni, Co, Rh, Nb, or Cr. Typical dielec. layers are prepd. from metal oxides, metal fluorides, **metal nitrides**, and metal carbides. Typical absorber layers are prepd. from Cr, Ni, Al, Pd, Pt, Ti, V, Co, Fe, Sn, W, Mo, Rh, Nb, C, graphite, Si, Ge, and compds., mixts., or alloys thereof. Typical luminescent materials are fluorescent dye-liq. cryst. polymer combination, cryst. phosphor, and solid or water-sol. quantum dot particles,.

IT **7429-90-5**, Aluminum, uses **7429-90-5D**, Aluminum, compds.
10043-11-5, Boron nitride, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(in luminescent multilayer pigments and films with color-shifting properties)

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 12 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:368853 HCAPLUS
DN 136:378422
TI **Epitaxial growth** of nitride compound semiconductor having reduced dislocation d.
IN Tsai, Tzong-Liang; Chang, Chih-Sung
PA United Epitaxy Company, Ltd., Taiwan
SO U.S. Pat. Appl. Publ., 12 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002056840	A1	20020516	US 2000-750351	20001229
	US 6462357	B2	20021008		
	US 6504183	B1	20030107	US 2000-659015	20000908
	JP 2002170991	A2	20020614	JP 2001-11695	20020614
PRAI	TW 2000-89124233	A	20001116		

AB The present invention provides materials and structures to reduce dislocation d. when growing a III-nitride compd. semiconductor. A II-nitride compd. single crystal-island layer is included in the semiconductor structure, and III-nitride compd. semiconductor layers are to grow thereon. It reduces the dislocation d. resulted from the difference between the lattice consts. of the GaN compd. semiconductor layers and the substrate. It also improves the crystn. property of the III-nitride compd. semiconductor.

L44 ANSWER 13 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:319786 HCAPLUS
DN 137:177265
TI Growth of GaN on Si(100) substrates using BP as a **buffer**

layer - selective **epitaxial growth**
AU Nishimura, Suzuka; Hanamoto, Hidetoshi; Terashima, Kazutaka; Matsumoto, Satoru
CS Faculty of Science and Technology, Keio University, Yokohama, Kanagawa, 223-8522, Japan
SO Materials Science & Engineering, B: Solid-State Materials for Advanced Technology (2002), B93(1-3), 135-138
CODEN: MSBTEK; ISSN: 0921-5107
PB Elsevier Science B.V.
DT Journal
LA English
AB A BP **buffer layer** was grown on Si(100) substrates by using halide VPE (HVPE) technique, and a uniform and continuous BP layer was successfully grown monocryst. on the window area. The roughness of the BP surface is much improved at the area grown over SiO2, which was confirmed by AFM observation. The growth of GaN was carried out by **metal** org. CVD (MOCVD) on normal BP/Si. The selective **epitaxial growth** is possible on Si(100) substrates using a SiO2 as a mask material. The results of selective growth and roughness are discussed.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 14 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:290769 HCAPLUS
DN 136:302792
TI Composite silicon-**metal nitride** barrier to prevent formation of metal fluorides in copper damascene
IN Chooi, Simon; Gupta, Subhash; Zhou, Mei-Sheng; Hong, Sangki
PA Chartered Semiconductor Manufacturing Ltd., Singapore
SO U.S., 16 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6372636	B1	20020416	US 2000-587467	20000605
	US 2002064941	A1	20020530	US 2002-43604	20020114
	US 6465888	B2	20021015		
PRAI	US 2000-587467	A3	20000605		

AB A method of forming amorphous silicon spacers followed by the forming of **metal nitride** over the spacers in a copper damascene structure (single, dual, or multi-structure) is disclosed in order to prevent the formation of fluorides in copper. In a first embodiment, the interconnection between the copper damascene and an underlying copper **metal layer** is made by forming an opening from the dual damascene structure to the underlying copper layer after the formation of the **metal nitride** layer over the amorphous silicon spacers formed on the inside walls of the dual damascene structure. In the second embodiment, the interconnection between the dual damascene structure and the underlying copper line is made from the dual damascene structure by etching into the underlying copper layer after the forming of the amorphous silicon spacers and before the forming of the **metal nitride** layer. In the third embodiment, the ternary metal silicon nitride spacer is formed by etching after having first formed the amorphous silicon layer and the nitride layer, in that order, and then etching the passivation/barrier layer at the bottom of the damascene structure into the underlying copper layer. In all three embodiments, **metal nitride** reacts with amorphous silicon to form a ternary metal silicon nitride having an excellent property of adhering to

copper while at the same time for forming an excellent barrier to diffusion of copper.

IT **7429-90-5**, Aluminum, uses **10043-11-5**, Boron nitride, uses
RL: DEV (Device component use); USES (Uses)
(composite silicon-**metal nitride** barrier to prevent formation of metal fluorides in copper damascene)

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 15 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:276321 HCAPLUS
DN 136:302046
TI Method of **epitaxial growth** of high quality nitride layers on silicon substrates
IN Temkin, Henryk; Nikishin, Sergey A.
PA Texas Tech University, USA
SO PCT Int. Appl., 27 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2002029873	A1	20020411	WO 2001-US27743	20011002
	W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
	RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG				
	US 6391748	B1	20020521	US 2000-677762	20001003
	AU 2001094534	A5	20020415	AU 2001-94534	20011002
PRAI	US 2000-677762	A	20001003		
	WO 2001-US27743	W	20011002		

AB Al nitride, AlN, layers are grown on Si substrate using mol. beam epitaxial (MBE) growth. The AlN layer is initially grown by subjecting the Si substrate to background NH3 followed by repetitively alternating the flux of (1) Al without NH3 and (2) NH3 without Al. After the surface of the Si structure is sufficiently covered with AlN, the substrate is subjected to flux of NH3 and Al applied simultaneously to continue the **epitaxial growth** process. The process minimizes the formation of amorphous Si nitride, SiN, compds. on the surface of the substrate which form due to background nitrogen levels in the mol. beam **epitaxial growth** app. A surface free of amorphous Si nitride is necessary for the formation of high quality AlN. The AlN layer may be further used as a **buffer layer** for AlGaN/GaN growth. After the AlN layer is grown on the Si substrate, the Si structure may be subjected to a flux of Ga and nitrogen to form a layer of GaN.

IT **25617-97-4**, Gallium nitride (GaN)
RL: CPS (Chemical process); DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(growth of GaN layer on AlN layer on silicon substrates using MBE)

IT **7440-55-3**, Gallium, processes
RL: CPS (Chemical process); PEP (Physical, engineering or chemical process); PROC (Process)
(growth of GaN layer on AlN layer on silicon substrates using MBE)

IT **24304-00-5**, Aluminum nitride
RL: CPS (Chemical process); DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(method of **epitaxial growth** of high quality nitride layers on silicon substrates)
IT **7429-90-5**, Aluminum, processes
RL: CPS (Chemical process); PEP (Physical, engineering or chemical process); PROC (Process)
(method of **epitaxial growth** of high quality nitride layers on silicon substrates)
RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 16 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:152586 HCAPLUS
DN 136:377635
TI High temperature growth of InN on GaP(111)B substrate using a new two-step growth method
AU Bhuiyan, Ashraful G.; Yamamoto, A.; Hashimoto, A.; Ito, Y.
CS Department of Electrical & Electronics Engineering, Fukui University, Fukui, 910-8507, Japan
SO Journal of Crystal Growth (2002), 236(1-3), 59-65
CODEN: JCRGAE; ISSN: 0022-0248
PB Elsevier Science B.V.
DT Journal
LA English
AB High temp. growth of InN was studied on GaP(111)B substrate using a new two-step growth method by **metal** org. VPE. A single cryst. InN film with an excellent surface morphol. can be grown on GaP(111)B at high temp. (600-650.degree.) using a low temp. InN **buffer layer**. The low temp. InN **buffer layer** is grown at 450.degree., and then the temp. is raised to the **epitaxial growth** temp. (600-650.degree.) while continuing the growth. It is a very effective growth technique to obtain high temp. growth of InN using a low temp. **buffer layer** . The low temp. InN **buffer layer** was also needed to suppress the substrate surface nitridation during the growth at such high temp. The differences of this new two-step growth method from the conventional two-step growth method as well as their influences on the grown InN films are also discussed.
RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 17 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:924303 HCAPLUS
DN 136:46931
TI Methods for characterizing and reducing adverse effects of texture of semiconductor films
IN Morales, Guarionex; You, Lu; Huang, Richard J.; Chan, Simon; Hopper, Dawn
PA USA
SO U.S. Pat. Appl. Publ., 31 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2001053600	A1	20011220	US 2001-773312	20010131
PRAI US 2000-179274P	P	20000131		

AB Improved methods for manufg. semiconductor devices incorporating barrier layers at metal/dielec. interfaces include the use of N-rich plasma, ion

beam implantation and/or electromagnetic radiation to form regions of nitrided metal. The barrier layers decrease the diffusion of dopants such as F, phosphorous and B from the dielec. material into the metal, thereby decreasing the formation of metal salts. By decreasing the formation of metal salts, the barrier layers of this invention decrease the formation of voids and areas of delamination, and thereby decrease the loss of elec. reliability during manuf. and during use. Addnl. aspects of this invention include methods for monitoring the deposition of thin **metal films** using sheet resistance measurements, and further embodiments of this invention include methods for monitoring the surface texture of films that undergo phase transitions. Addnl. embodiments include methods for monitoring and calibrating the temps. of manufg. processes on the surfaces of semiconductor wafers. Thus, useful lifetimes of semiconductor devices can be increased, and the manuf. of reliable devices can be easier, less expensive and more reproducible.

IT **7429-90-5**, Aluminum, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(layer of; methods for characterizing and reducing adverse effects of texture of semiconductor films)

IT **24304-00-5**, Aluminum nitride
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(methods for characterizing and reducing adverse effects of texture of semiconductor films)

L44 ANSWER 18 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:844958 HCAPLUS
DN 135:379634
TI Diffusion barriers between noble metal electrodes and **metalization layers**, and integrated circuit and semiconductor devices comprising same
IN Kirlin, Peter S.; Summerfelt, Scott R.; Mcintryre, Paul
PA Advanced Technology Materials, Inc., USA
SO U.S., 19 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6320213	B1	20011120	US 1997-994089	19971219
PRAI US 1997-994089		19971219		

AB A dynamic random access memory device includes storage capacitors using a high dielec. const. material, such as, BaSrTiO3, SrBi2Ta2O9, and PbZrTiO3, for the capacitors' insulator. The device includes a conductive plug formed over and connecting with a semiconductor substrate. A **buffer layer** of Ti silicide lays over the plug, and this layer serves to trap dangling bonds and to passivate the underlying surface. A 1st diffusion barrier layer, e.g., Ti Al nitride, covers the Ti silicide. A capacitor 1st electrode lays over the diffusion barrier layer. The high dielec. const. material is laid over the capacitor 1st electrode. A capacitor 2nd electrode is laid over the high dielec. const. material. A 2nd diffusion barrier layer is deposited on the capacitor 2nd electrode. A conductor, such as Al, is laid over the 2nd diffusion barrier layer. An isolation dielec. can be deposited over the conductor at a high temp. without causing O or metallic diffusion through the 1st and 2nd diffusion barrier layers.

IT **7429-90-5**, Aluminum, uses
RL: DEV (Device component use); USES (Uses)
(capacitor electrode material; diffusion barriers between noble metal

electrodes and **metalization layers**, and integrated circuit and semiconductor devices comprising same)

IT **7440-55-3**, Gallium, uses **24304-00-5**, Aluminum nitride (AlN)
RL: DEV (Device component use); USES (Uses)
(diffusion barrier material; diffusion barriers between noble metal electrodes and **metalization layers**, and integrated circuit and semiconductor devices comprising same)

RE.CNT 19 THERE ARE 19 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 19 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:813467 HCAPLUS
DN 135:326051
TI Process for growing **gallium nitride** and its compound film
IN Han, Peide
PA Inst. of Semiconductors, Chinese Academy of Sciences, Peop. Rep. China
SO Faming Zhuanli Shenqing Gongkai Shuomingshu, 12 pp.
CODEN: CNXXEV
DT Patent
LA Chinese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI CN 1289866	A	20010404	CN 1999-119773	19990928
PRAI CN 1999-119773		19990928		

AB The process comprises two-step **epitaxial growing** of hexagonal GaN and its compd. film on homopolar c-Al2O3 matrix, polar hexagonal crystal matrix, or polar cubic and square crystal matrix by using **metal** org. CVD equipment. The epitaxial face of the homopolar c-Al2O3 matrix is the crystal face against the seed crystal face, that of polar hexagonal crystal matrix is its (000-1) face, and that of polar cubic and square crystal matrix is its (-1-1-1) face. The polar hexagonal crystal matrix is (000-1) 6H-SiC crystal or (000-1) ZnO crystal, and the polar cubic and square crystal matrix is (-1-1-1) GaAs crystal and (-1-1-1) MgAl2O4 crystal resp. The thickness of (000-1) GaN **buffer layer** is greater than the surface roughness of the matrix. The improved Hall coeff. and photoluminescence properties are reported.

L44 ANSWER 20 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:788743 HCAPLUS
DN 135:337211
TI Method and apparatus for **epitaxial growth** of Group IIIA **metal nitride** on single crystal substrate
IN Kong, Chih-rong
PA Kuangka Optoelectric Co., Ltd., Taiwan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2001302398	A2	20011031	JP 2000-106482	20000407
PRAI JP 2000-106482		20000407		

AB A single crystal substrate is washed, dried, placed in an epitaxy app., heated to a temp., subjected to chem. adsorption of Group IIIA metal by supplying an organometallic compd. **gas** contg. the metal, and subjected to epitaxy under reaction of the metal and N from a N-contg.

gas supplied on the substrate. The method may involve plurality of chem. adsorption steps and epitaxy steps for forming a multilayer structure. The method is suitable for prepn. of multilayer structure of multiple quantum well, light-emitting diode, laser diode, optical sensor, or high-power transistor. The app. for manuf. of the multilayer structure for photoelec. device is also claimed.

L44 ANSWER 21 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:709864 HCAPLUS
DN 135:250364
TI A semiconductor device, a method for manufacturing a semiconductor device, and an **epitaxial growth** substrate for a semiconductor device from **aluminum gallium indium nitride**
IN Shibata, Tomohiko; Asai, Keiichiro; Nagai, Teruyo; Tanaka, Mitsuhiro
PA NGK Insulators, Ltd., Japan
SO Eur. Pat. Appl., 9 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1137077	A2	20010926	EP 2001-106478	20010322
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 2001338886	A2	20011207	JP 2001-54786	20010228
	US 2002028343	A1	20020307	US 2001-812618	20010320
	US 6492191	B2	20021210		
	CN 1316783	A	20011010	CN 2001-116499	20010323
PRAI	JP 2000-84064	A	20000324		
	JP 2001-54786	A	20010228		

AB A semiconductor device has a substrate body, an AlxGayInzN (x+y+z = 1,x,y,z.gtoreq.0) film **epitaxially grown** direct on the substrate body or **epitaxially grown** via a **buffer layer** on the substrate body, and a **metal** film provided on the rear surface of the substrate body. In the case of the manufg. the semiconductor device, the substrate body is heated, by a heater, uniformly and efficiently through the thermal radiation of the heater.

L44 ANSWER 22 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:684335 HCAPLUS
DN 135:219189
TI Growth of **metal nitrides** by reactive MBE using ammonia
AU Parkhomovsky, Alexander
CS Univ. of Minnesota, Minneapolis, MN, USA
SO (2000) 100 pp. Avail.: UMI, Order No. DA9991442
From: Diss. Abstr. Int., B 2001, 61(10), 5512
DT Dissertation
LA English
AB Unavailable

L44 ANSWER 23 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:594300 HCAPLUS
DN 135:145011
TI Procedure for the epitaxy of single-crystal aluminum nitride layers
IN Lebedev, Vadim; Richter, Wolfgang
PA Germany
SO Ger. Offen., 6 pp.
CODEN: GWXXBX

DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 10006108	A1	20010816	DE 2000-10006108	20000211
PRAI	DE 2000-10006108		20000211		

AB The task of the invention a procedure for the epitaxial deposition of single-crystal, domain-free AlN layers on Si(001)-substrates. A Si(001) off-axis substrate is used, with its (001)-surface tilted a few degrees in the <110> direction. The Si surface is prepd. at a temp. .gtoreq. 1100.degree. so that a terrace structure with at. double layer steps develops, with the step edges running parallel to the <-110> direction. Then, an 2-monolayer thick Al layer is vapor deposited at low substrate temp., and by subsequent introduction of N2, epitaxial AlN is afforded. During the **epitaxial growth** of AlN the substrate temp. is gradually increased to the optimal epitaxy temp. The single-domain AlN layers on Si(001)-wafers can be used for acoustic surface wave components and as **buffer layers** for the epitaxy of GaN semiconductor components.

IT **7429-90-5**, Aluminum, processes
RL: PEP (Physical, engineering or chemical process); RCT (Reactant); TEM (Technical or engineered material use); PROC (Process); RACT (Reactant or reagent); USES (Uses)
(procedure for epitaxy of single-crystal aluminum nitride layers)

IT **24304-00-5P**, Aluminum nitride
RL: SPN (Synthetic preparation); TEM (Technical or engineered material use); PREP (Preparation); USES (Uses)
(procedure for epitaxy of single-crystal aluminum nitride layers)

L44 ANSWER 24 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:538669 HCAPLUS
DN 135:325006
TI Conventional and pendeo-**epitaxial growth** of GaN(0001) thin films on Si(111) substrates
AU Davis, R. F.; Gehrke, T.; Linthicum, K. J.; Preble, E.; Rajagopal, P.; Ronning, C.; Zorman, C.; Mehregany, M.
CS Department of Materials Science and Engineering, North Carolina State University, Raleigh, NC, 27695-7907, USA
SO Journal of Crystal Growth (2001), 231(3), 335-341
CODEN: JCRGAE; ISSN: 0022-0248
PB Elsevier Science B.V.
DT Journal
LA English

AB Single-crystal wurtzitic GaN(0001) films have been grown via conventional methods on high-temp. AlN(0001) **buffer layers** previously deposited on 3C-SiC(111)/Si(111) substrates using **metal** org. vapor phase epitaxy (MOVPE). Formation of the 3C-SiC transition layer employed a carburization step and the subsequent deposition of epitaxial 3C-SiC(111) on the Si(111) surface using atm. pressure chem. vapor deposition (APCVD) for both processes. Similar films, except with significantly reduced dislocation densities, have been grown via pendeo-epitaxy (PE) from the (1120) sidewalls of silicon nitride masked, raised, rectangular, and [1 100] oriented GaN stripes etched from films conventionally grown on similarly prepd., Si-based, multilayer substrates. The FWHM of the (0002) X-ray diffraction peak of the conventionally grown GaN was 1443 arcsec. The FWHM of the photoluminescence (PL) spectra for the near band-edge emission on these films was 19 meV. Tilting in the coalesced PE-grown GaN epilayers of 0.2.degree. was confined to the areas of lateral overgrowth over the masks; no tilting was obsd. in the material suspended above the trenches. The strong, low-temp. PL band-edge peak at

3.456 eV with an FWHM of 17 meV in the PE films was comparable to that obsd. in PE GaN films grown on AlN/6H-SiC(0001) substrates.
RE.CNT 26 THERE ARE 26 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 25 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:342995 HCAPLUS
DN 135:99991
TI Improved heteroepitaxial MBE GaN growth with a Ga metal **buffer layer**
AU Kim, Yihwan; Subramanya, Sudhir G.; Krueger, Joachim; Siegle, Henrik; Shapiro, Noad; Armitage, Robert; Feick, Henning; Weber, Eicke R.; Kisielowski, Christian; Yang, Yi; Cerrina, Franco
CS Department of Materials Science and Engineering, University of California at Berkeley, Berkeley, CA, 94720, USA
SO Materials Research Society Symposium Proceedings (2001), 622(Wide-Bandgap Electronic Devices), T4.10.1-T4.10.6
CODEN: MRSPDH; ISSN: 0272-9172
PB Materials Research Society
DT Journal
LA English
AB The use of pure Ga as a **buffer layer** results in improved crystal quality of GaN epilayers grown by plasma-assisted MBE on c-plane sapphire. The resulting epilayers show electron Hall mobilities .ltoreq.400 cm2/Vs at a background carrier concn. of 4 .times. 1017 cm-3, an outstanding value for an MBE-grown GaN layer on sapphire. Structural properties are also improved; the asym. (101) x-ray rocking curve width is drastically reduced with respect to that of the ref. GaN epilayer grown on a low-temp. GaN **buffer layer**. Nitrided Ga **metal layers** were studied for different Ga deposition time. These layers can be regarded as templates for the subsequent Ga main layer growth. There is an optimum Ga **metal layer** deposition time for improving the electron mobility in the epilayer. Heating of the Ga **metal layer** to the epilayer growth temp. under N plasma is sufficient to produce highly oriented GaN crystals. However, nonuniform surface morphol. and incomplete surface coverage were obsd. after nitridation of comparatively thick Ga **metal layers**. This is the reason for the decreasing electron mobility of the epilayers as the Ga **metal layer** thickness exceeds the optimum value.
IT **7440-55-3**, Gallium, properties
RL: MOA (Modifier or additive use); PEP (Physical, engineering or chemical process); PRP (Properties); PROC (Process); USES (Uses)
(improved plasma-assisted MBE GaN growth with Ga metal **buffer layer** on sapphire)
IT **25617-97-4**, Gallium nitride (GaN)
RL: PEP (Physical, engineering or chemical process); PRP (Properties); PROC (Process)
(improved plasma-assisted MBE GaN growth with Ga metal **buffer layer** on sapphire)
RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 26 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:325060 HCAPLUS
DN 134:346596
TI **Epitaxial growth** and stabilization of transition **metal nitride**-based superlattices and **buffer layers**
AU Kim, Ilwon
CS Northwestern Univ., Evanston, IL, USA

SO (2000) 222 pp. Avail.: UMI, Order No. DA9974303
From: Diss. Abstr. Int., B 2000, 61(6), 3234
DT Dissertation
LA English
AB Unavailable

L44 ANSWER 27 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:280817 HCAPLUS
DN 134:287668
TI Gallium nitride type compound semiconductor LED
IN Hata, Toshio; Morimoto, Taiji; Kamikawa, Takeshi; Yamamoto, Kensaku
PA Sharp Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001111109	A2	20010420	JP 1999-286326	19991007
	TW 465128	B	20011121	TW 2000-89120901	20001006
PRAI	JP 1999-286326	A	19991007		

AB The LED comprises: (1) a sapphire substrate; (2) an n-GaN **buffer** /contact layer having (3) an n shoulder electrode; (4) a p-GaN layer; (5) a thin **metal layer** having (6) a p shoulder electrode; and (7) a metal oxide and (8) a phosphor layer for converting the LED light, where (5) is 1-10 nm thick; and (7) is 0.1-1 .mu.m thick and comprises In2O3, SnO2, ZnO, Cd2SnO4 or CdSnO3.
IT **25617-97-4**, Gallium nitride (GaN)
RL: DEV (Device component use); USES (Uses)
(gallium nitride type compd. semiconductor LED)
IT **7429-90-5**, Aluminum, uses
RL: DEV (Device component use); MOA (Modifier or additive use); USES (Uses)
(gallium nitride type compd. semiconductor LED)

L44 ANSWER 28 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:276896 HCAPLUS
DN 135:84730
TI Influence of the AlN **buffer layer** growth on AlGaN/GaN films deposited on (1 1 1)Si substrates
AU Liaw, H. M.; Venugopal, R.; Wan, J.; Melloch, M. R.
CS Semiconductor Products Sector, Compound Semiconductor Technologies, 2100 E. Elliot Road, EL 740, Motorola Inc., Tempe, AZ, 85284, USA
SO Solid-State Electronics (2001), 45(3), 417-421
CODEN: SSELA5; ISSN: 0038-1101
PB Elsevier Science Ltd.
DT Journal
LA English
AB Use of an AlN **buffer layer** is an enabling technique for the **epitaxial growth** of GaN on Si(1 1 1) substrates. The AlN growth temp. is a significant factor that affects the properties of the GaN film and the AlGaN/GaN heterostructure. The AlN **buffer** grown at 1155.degree. exhibited a uniform sized, preferred-oriented and highly faceted grain microstructure that led to subsequently grown AlGaN/GaN films with better quality than those on the AlN **buffer** grown at other temps. The AlGaN/GaN film quality evaluations included photoluminescence properties, surface planarity, Hall mobility and film strain.
IT **24304-00-5**, Aluminum nitride (AlN)
RL: PEP (Physical, engineering or chemical process); TEM (Technical or

engineered material use); PROC (Process); USES (Uses)
(influence of aluminum nitride **buffer layer** growth on aluminum gallium nitride/gallium nitride films deposited on (1 1 1)Si substrates)

IT **7429-90-5**, Aluminum, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(outdiffusion; influence of aluminum nitride **buffer layer** growth on aluminum gallium nitride/gallium nitride films deposited on (1 1 1)Si substrates)

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 29 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:228513 HCAPLUS
DN 134:260043
TI Field-effect transistor and fabrication of same.
IN Ohno, Yasuo; Kasahara, Kensuke; Kunihiro, Kazuaki; Takahashi, Hiroyuki; Nakayama, Tatsumine; Haneyama, Nobuyuki
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2001085670	A2	20010330	JP 1999-259681	19990914
PRAI JP 1999-259681		19990914		

AB The field-effect transistor includes GaN layer or InGaN layer as channel layer, an n-type or nondoped AlGaN charge-supply layer formed on the channel layer, a **metal layer** formed on the charge-supply layer, an insulator layer formed on the **metal layer**, an opening formed on the insulator layer and the **metal layer**, an insulating film formed on the side wall of the opening, and a metal gate electrode deposited in the opening. The above stated **metal layer** is formed from Ti layer and Al layer. The above stated channel layer may be formed on sapphire or SiC substrate via an AlGaN **buffer layer**.

IT **25617-97-4**, Gallium nitride (GaN)
RL: DEV (Device component use); USES (Uses)
(channel; field-effect transistor and fabrication of same)

IT **7429-90-5**, Aluminum, uses
RL: DEV (Device component use); USES (Uses)
(field-effect transistor and fabrication of same)

IT **7440-42-8**, Boron, uses
RL: MOA (Modifier or additive use); USES (Uses)
(field-effect transistor and fabrication of same)

L44 ANSWER 30 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:185242 HCAPLUS
DN 134:215182
TI Epitaxy of semiconductor
IN Wang, Wang Nang; Shreter, Yurii Georgievich; Rebane, Yurii Toomasovich
PA Arima Optoelectronics Corp., Taiwan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI	JP 2001068414	A2	20010316	JP 2000-206498	20000707
	GB 2354370	A1	20010321	GB 2000-16039	20000629
	GB 2354370	B2	20010905		
	CN 1281247	A	20010124	CN 2000-120258	20000714
	US 6380050	B1	20020430	US 2000-616725	20000714
	TW 475208	B	20020201	TW 2000-89114971	20000726
PRAI	GB 1999-16549	A	19990714		
	GB 2000-16039	A	20000629		

AB A method for **epitaxially growing** a semiconductor such as AlN, GaN, or InN on a lattice-mismatched substrate such as sapphire or SiC using a **buffer layer** having a solid-liq. phase transition involves **epitaxially growing** the **buffer layer** on the substrate at a temp. lower than the m.p. of the **buffer layer**, **epitaxially growing** a protective layer having a m.p. higher than the growth temp. of the semiconductor at a temp. lower than the m.p. of the **buffer layer**, and **epitaxially growing** the semiconductor to the thickness larger than that of the protective layer at a temp. higher than the m.p. of the **buffer layer**. Specifically, the **buffer layer** may comprise aluminum, copper, magnesium, lead, gold, silver, or their alloys, and the protective layer may comprise MgO, alumina, AlN, GaN, or InN.

IT **7429-90-5**, Aluminum, uses
RL: NUU (Other use, unclassified); USES (Uses)
(epitaxy of semiconductor)

IT **24304-00-5**, Aluminum nitride (AlN) **25617-97-4**, Gallium nitride (GaN) **25617-98-5**, Indium nitride (InN)
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(epitaxy of semiconductor)

L44 ANSWER 31 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:103944 HCAPLUS
DN 134:201421
TI Elastic strain relief in nitridated **Ga metal** **buffer layers** for epitaxial GaN growth
AU Kim, Yihwan; Shapiro, Noad A.; Feick, Henning; Armitage, Robert; Weber, Eicke R.; Yang, Yi; Cerrina, Franco
CS Department of Materials Science and Engineering, and Materials Science Division, University of California at Berkeley, Lawrence Berkeley National Laboratory, Berkeley, CA, 94720, USA
SO Applied Physics Letters (2001), 78(7), 895-897
CODEN: APPLAB; ISSN: 0003-6951
PB American Institute of Physics
DT Journal
LA English
AB GaN epitaxial layers were grown on sapphire by MBE using nitrided **Ga** films as **buffer layers**. The mech. properties of the **buffer layers** were studied and correlated with their chem. compn. as detd. by synchrotron radiation photoelectron spectroscopy. Biaxial tension expts. were performed by bending the substrates in a pressure cell designed for simultaneous photoluminescence measurements. The shift of the excitonic luminescence peak was used to det. the stress induced in the main GaN epilayer. The fraction of stress transferred from substrate to main layer was as low as 27% for samples grown on nitrided **metal buffer layers**, compared to nearly 100% for samples on conventional low-temp. GaN **buffer layers**. The efficiency of stress relief increased in proportion to the fraction of metallic **Ga** in the nitrided **metal buffer layers**. These findings suggest GaN films contg. residual metallic **Ga** may serve

as compliant **buffer layers** for heteroepitaxy.

IT **7440-55-3, Gallium**, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(elastic strain relief in nitrided **gallium buffer layers** for epitaxial **gallium nitride** growth)

IT **25617-97-4P, Gallium nitride** (GaN)
RL: PNU (Preparation, unclassified); PRP (Properties); PREP (Preparation)
(elastic strain relief in nitrided **gallium buffer layers** for **epitaxial growth** of)

RE.CNT 18 THERE ARE 18 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 32 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:728930 HCAPLUS
DN 134:31998
TI Preparation of **metal nitride** and oxide thin films using shielded reactive vacuum arc deposition
AU Miyano, R.; Kimura, K.; Izumi, K.; Takikawa, H.; Sakakibara, T.
CS Department of Electrical and Electronic Engineering, Toyohashi University of Technology, Toyohashi, 441-8580, Japan
SO Vacuum (2000), 59(1), 159-167
CODEN: VACUAV; ISSN: 0042-207X
PB Elsevier Science Ltd.
DT Journal
LA English
AB Various **metal nitride** and oxide thin films were prepd. using a shielded reactive vacuum arc deposition. The cathode materials used as metal ion sources were Al, Ti, Cu, Cr, and Zn. These nitride and oxide films were deposited in pure N2 and O2 gas flows, resp. First, the films were deposited for a short period by both non-shielded and shielded methods, and the macrodroplet appearance on the films was compared. Macrodroplets were reduced remarkably, to less than one-hundredth for Al in N2, Zn in N2 and Al in O2. For Ti in N2, Cr in N2, Cu in N2, Ti in O2, and Zn in O2, the macrodroplets were reduced by one-third, although they were not reduced for Cr in O2. X-ray diffraction anal. revealed that crystd. films were AlN, TiN, CrN, Cu3N with Cu, CuO, and ZnO, and that amorphous films were Al2O3, TiO2 and Cr oxide. Zn3N2 were weakly synthesized in Zn **metal film**. AlN, Al2 O3 and TiO2 films were very transparent with refractive indexes of 2.1, 1.6 and 2.3 at 500 nm, resp. ZnO film also exhibited good transparency.

IT **24304-00-5P**, Aluminum nitride
RL: PNU (Preparation, unclassified); PRP (Properties); PREP (Preparation)
(prepn. of **metal nitride** and oxide thin films using shielded reactive vacuum arc deposition in pure N2 and O2 flows using Al, Ti, Cu, Cr, and Zn as metal sources)

IT **7429-90-5**, Aluminum, reactions
RL: RCT (Reactant); RACT (Reactant or reagent)
(prepn. of **metal nitride** and oxide thin films using shielded reactive vacuum arc deposition in pure N2 and O2 flows using Al, Ti, Cu, Cr, and Zn as metal sources)

RE.CNT 13 THERE ARE 13 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 33 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:663677 HCAPLUS
DN 133:230194
TI GaN-type semiconductor light-emitting devices
IN Sendai, Toshiaki; Shibata, Naoki; Ito, Jun; Noiri, Shizuyo
PA Toyota Gosei Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.

CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 3

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000261032	A2	20000922	JP 1999-58128	19990305
	EP 1039555	A1	20000927	EP 2000-104655	20000303
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	US 2003042505	A1	20030306	US 2001-20460	20011218
PRAI	JP 1999-58128	A	19990305		
	JP 1999-60206	A	19990308		
	JP 1999-61155	A	19990309		
	JP 1999-90833	A	19990331		
	JP 1999-235450	A	19990823		
	US 2000-518724	A3	20000303		

AB The devices typically comprise: an n electrode; a Si substrate; an Al **buffer layer**; a (Ti,Zr)N layer; a GaInN-QW/GaN-barrier MQW layer; a p-GaN cladding layer; and a p electrode.

IT **7429-90-5**, Aluminum, uses **25617-97-4**, Gallium nitride (GaN)
RL: DEV (Device component use); USES (Uses)
(GaN-type semiconductor light-emitting devices)

L44 ANSWER 34 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:483168 HCAPLUS
DN 133:197103
TI Enhanced adhesion through local epitaxy of transition-**metal nitride** coatings on ferritic steel promoted by metal ion etching in a combined cathodic arc/unbalanced magnetron deposition system
AU Schonjahn, C.; Donohue, L. A.; Lewis, D. B.; Munz, W.-D.; Twesten, R. D.; Petrov, I.
CS Materials Research Institute, Sheffield Hallam University, Sheffield, S11WB, UK
SO Journal of Vacuum Science & Technology, A: Vacuum, Surfaces, and Films (2000), 18(4, Pt. 2), 1718-1723
CODEN: JVTAD6; ISSN: 0734-2101
PB American Institute of Physics
DT Journal
LA English
AB In situ substrate cleaning by ion etching prior to deposition in phys. vapor deposition processes is a key step in achieving good film adhesion, which is essential for all coating applications. Irradn. with metal or **gas** ions alters substrate surface chem., topog., and microstructure thus affecting subsequent film growth. This study compares Ti1-xAlxN/ferritic steel (x = 0.54) interfaces formed after Cr ion bombardment at neg. substrate biases, Us, ranging from 600 to 1200 V during a Cr cathodic arc discharge, stabilized with a 0.06 Pa Ar background pressure. Samples biased with -1200 V in an Ar glow discharge at a pressure of 0.6 Pa were also investigated. Microstructure and microchem. of the interfaces was studied by scanning transmission electron microscopy with energy dispersive x-ray anal. using cross-sectional samples. Cr ion etching with Us = 1200 V resulted in a net removal of over 100 nm of substrate material with the formation, through implantation, of a Cr-enriched near-surface region extending to a depth of .apprx.10 nm. As Us was reduced to 600 V, Cr accumulated at the surface as a .gtorsim.5 nm thick layer. Ar was incorporated at the surface to levels of 4-6 at.% during both Cr arc and Ar glow discharge etching. The microstructure of Ti1-xAlxN overlayers was dramatically affected by pretreatment procedures. Ar sputter cleaned steel surfaces (Us = 1200 V)

promote nucleation of randomly oriented grains leading to a competitive column growth with small column size and open boundaries. In contrast, Cr irradn. at the same bias voltage results in local **epitaxial growth** of Ti1-xAlxN on steel and lead to a superior performance in scratch testing compared to coatings deposited after Cr treatment with Us = 600 V or Ar ion bombardment at Us = 1200 V. Crit. loads were 63, 47, and 27 N, resp.

RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 35 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:387846 HCAPLUS
DN 133:127987
TI Using statistical experimental design to investigate the role of the initial growth conditions on GaN epitaxial films grown by molecular beam epitaxy
AU Lee, Kyeong K.; Doolittle, William A.; Brown, April S.; May, Gary S.; Stock, Stuart R.
CS School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, 30332-0250, USA
SO Journal of Vacuum Science & Technology, B: Microelectronics and Nanometer Structures (2000), 18(3), 1448-1452
CODEN: JVTBD9; ISSN: 0734-211X
PB American Institute of Physics
DT Journal
LA English
AB The nucleation and **buffer** growth of GaN on (0001) sapphire by mol. beam epitaxy are investigated using the design of expts. approach. Six factors are simultaneously varied: time and temp. for nitridation, **buffer** growth temp., Ga cell temp., growth time, and nitrogen plasma power during **buffer** growth. In situ RHEED is utilized to monitor these steps. The quality of the epitaxial layers obtained is examd. by means of electron mobility and at. force microscopy. It is shown that the **buffer layer** growth rate has the greatest influence on improving the elec. properties of the subsequent GaN epitaxial layer. Depending on the growth conditions, the Hall mobility of the GaN epitaxial layer varies from 24 to 238 cm2/V s. Changes in surface morphol. are correlated with improvements in electron mobility. We also discuss interaction effects between the factors. A trend extd. from a least-squares model reveals that 300 K Hall mobility is greatly improved at high growth rate and low nitrogen plasma power during **buffer** growth.
IT **25617-97-4P**, Gallium nitride
RL: PEP (Physical, engineering or chemical process); PNU (Preparation, unclassified); TEM (Technical or engineered material use); PREP (Preparation); PROC (Process); USES (Uses)
(using statistical exptl. design to investigate the role of the initial growth conditions on GaN epitaxial films grown by mol. beam epitaxy)
IT **7440-55-3**, Gallium, reactions
RL: RCT (Reactant); RACT (Reactant or reagent)
(using statistical exptl. design to investigate the role of the initial growth conditions on GaN epitaxial films grown by mol. beam epitaxy)
RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 36 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:373386 HCAPLUS
DN 133:11124
TI Growth of crack-free thick AlGaN layer and its application to GaN-based laser diode
AU Akasaki, I.; Kamiyama, S.; Detchprohm, T.; Takeuchi, T.; Amano, H.

CS Department of Electrical and Electronic Engineering, High-Tech Research center, Meijo University, Nagoya, 468-8502, Japan
SO Materials Research Society Symposium Proceedings (2000), 595(GaN and Related Alloys--1999), W6.8.1-W6.8.6
CODEN: MRSPDH; ISSN: 0272-9172
PB Materials Research Society
DT Journal
LA English
AB In the field of group-III nitrides, hetero-**epitaxial growth** was one of the most important key technologies. A thick layer of AlGaN alloy with higher AlN molar fraction is difficult to grow on sapphire substrate, because the alloy layer is easily cracked. Probably one cause of generating cracks is a large lattice mismatch between an AlGaN and a GaN, when AlGaN is grown on the underlying GaN layer. The authors have achieved crack-free Al0.07Ga0.93N layer with the thickness of >1.mu.m using underlying Al0.05Ga0.95N layer. The underlying Al0.05Ga0.95N layer was grown directly on sapphire by using the low-temp.-deposited **buffer layer** (LT-**buffer layer**). Since a lattice mismatch between the underlying Al0.05Ga0.95N layer and upper Al0.07Ga0.93N layer is relatively small, the generation of cracks probably is suppressed. This technol. is applied to a GaN-based laser diode structure, in which thick n-Al0.07Ga0.93N cladding layer grown on the Al0.05Ga0.95N layer, improves optical confinement and single-robe far field pattern in vertical direction.
RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 37 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:306756 HCAPLUS
DN 132:327806
TI Pendeo-**epitaxial growth** of **gallium nitride** on silicon substrates
AU Gehrke, Thomas; Linthicum, Kevin J.; Preble, Edward; Rajagopal, Pradeep; Ronning, Carsten; Zorman, Christian; Mehregany, Mehran; Davis, Robert F.
CS Department of Materials Science and Engineering, North Carolina State University, Raleigh, NC, USA
SO Journal of Electronic Materials (2000), 29(3), 306-310
CODEN: JECMA5; ISSN: 0361-5235
PB Minerals, Metals & Materials Society
DT Journal
LA English
AB Pendeo-epitaxy (PE) from raised, [0001] oriented GaN stripes covered with Si3N4 masks was employed for the growth of coalesced films of GaN(0001) with markedly reduced densities of line and planar defects on Si(111)-based substrates. Each substrate contained previously deposited 3C-SiC(111) and AlN(0001) transition layers and a GaN seed layer from which the stripes were etched. The 3C-SiC transition layer eliminated chem. reactions between the Si and the NH3 and the **Ga metal** from the decompn. of Et3Ga. The 3C-SiC and the GaN seed layers, each 0.5 .mu.m thick, were also used to minimize the cracking and warping of the GaN/SiC/Si assembly caused primarily by the stresses generated on cooling due to the mismatches in the coeffs. of thermal expansion. Tilting in the coalesced GaN epilayers of 0.2.degree. was confined to areas of lateral overgrowth over the masks; no tilting was obsd. in the material suspended above the trenches. The strong, low-temp. PL band-edge peak at 3.456 eV with a FWHM of 17 meV was comparable to that obsd. in PE GaN films grown on AlN/6H-SiC(0001) substrates.
RE.CNT 28 THERE ARE 28 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 38 OF 67 HCAPLUS COPYRIGHT 2003 ACS

AN 2000:134757 HCAPLUS
DN 132:200554
TI **Epitaxial growth** of wurtzite GaN on Si(111) by a vacuum reactive evaporation
AU Zhang, Haoxiang; Ye, Zhizhen; Zhao, Binghui
CS State Key Laboratory of Silicon Materials, Zhejiang University, Hangzhou, 310027, Peop. Rep. China
SO Journal of Applied Physics (2000), 87(6), 2830-2834
CODEN: JAPIAU; ISSN: 0021-8979
PB American Institute of Physics
DT Journal
LA English
AB A single cryst. GaN film on Si(111) with a GaN **buffer layer** is grown by a simple reactive evapn. method. SEM, XRD, TEM, photoluminescence measurement (PL), and Hall measurement results indicate that the single cryst. wurtzite GaN was successfully grown on the microcryst. GaN **buffer layers** on Si(111) substrate. The surface of the GaN films is mirror-like and crack-free. A pronounced GaN (0002) peak appears in the XRD pattern. The full width at half max. (FWHM) of the double-crystal x-ray rocking curve for (0002) diffraction from the GaN epilayer is 30 arcmin. The TEM reveals that a 10. nm GaN **buffer layer** in the microcryst. state exists between the Si substrate and the epilayer, which dissipates most of the stress energy. The PL spectrum shows that the GaN epilayer emits light at the wavelength of 365 nm with a FWHM of 8 nm (74.6 meV). The unintentionally doped films were n type with a carrier concn. of 1.76 .times. 1018/cm3 and an electron mobility of 142 cm3/V s. The growth technique described is simple but very powerful for growing single cryst. GaN films on Si substrates.
IT **25617-97-4P**, Gallium nitride
RL: PEP (Physical, engineering or chemical process); PRP (Properties); SPN (Synthetic preparation); PREP (Preparation); PROC (Process)
(**epitaxial growth** of wurtzite GaN on Si(111) by a vacuum reactive evapn.)
IT **7440-55-3**, Gallium, reactions
RL: RCT (Reactant); RACT (Reactant or reagent)
(**epitaxial growth** of wurtzite GaN on Si(111) by a vacuum reactive evapn. with nitridation of substrate)
RE.CNT 19 THERE ARE 19 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 39 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:756963 HCAPLUS
DN 131:353721
TI Manufacture of thin polycrystalline silicon films and the films
IN Yamada, Takumi; Yamada, Takeshi; Nishioka, Takashi; Tachikawa, Masami; Kawakami, Takeshi
PA Nippon Telegraph and Telephone Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11330519	A2	19991130	JP 1999-4988	19990112
PRAI	JP 1998-22837		19980119		

AB The thin polycryst. Si films are prepd. by forming a Si nitride or **metal nitride** film on a substrate, forming a **metal film** on the nitride film, and forming Si film on the heated **metal film**. An intermediate Si layer may be formed between the nitride film and the **metal film**.

The Si films are useful for solar cells.
IT **7429-90-5**, Aluminum, uses **24304-00-5**, Aluminum nitride
RL: NUU (Other use, unclassified); USES (Uses)
(covering of substrates with nitride and **metal layers** in thin polycryst. silicon film manuf. for solar cells)

L44 ANSWER 40 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:591122 HCAPLUS
DN 131:331211
TI Use of magnetocrystalline anisotropy in spin-dependent tunneling
AU Lukaszew, R. A.; Sheng, Y.; Uher, C.; Clarke, R.
CS Randall Laboratory of Physics, University of Michigan, Ann Arbor, MI, 48109-1120, USA
SO Applied Physics Letters (1999), 75(13), 1941-1943
CODEN: APPLAB; ISSN: 0003-6951
PB American Institute of Physics
DT Journal
LA English
AB **Epitaxial growth** techniques are used to impose in-plane magnetocryst. anisotropy on a spin-polarized tunneling configuration. A Cu(100) **buffer layer** grown on a Si(100) substrate stabilizes epitaxial fcc. Co as one of the ferromagnetic electrodes. The neg. magnetocryst. const. of this metastable phase favors easy axes along Co .ltbbrac.110.rtbbrac. and, due to the single crystal nature of this layer, the coercivity is more than an order of magnitude larger than in the polycryst. layers which form the 2nd electrode. The approach provides a way to access the high degree of spin polarization characteristic of the 3d transition **metals**.
RE.CNT 17 THERE ARE 17 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 41 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:418266 HCAPLUS
DN 131:207071
TI Selected energy epitaxial deposition of GaN and AlN on SiC(0001) using seeded supersonic free jets of NH3 in helium
AU Torres, V. M.; Doak, R. B.; Wilkens, B. J.; Smith, D. J.; Tsong, I. S. T.
CS Department of Physics and Astronomy, Arizona State University, Tempe, AZ, 85287-1504, USA
SO Journal of Vacuum Science & Technology, A: Vacuum, Surfaces, and Films (1999), 17(4, Pt. 1), 1570-1576
CODEN: JVTAD6; ISSN: 0734-2101
PB American Institute of Physics
DT Journal
LA English
AB By expanding a **gas** mixt. into vacuum through a supersonic nozzle, a heavy seed species in a light diluent **gas** can be aerodynamically accelerated to suprathermal translational energies. Such beams are intense, directional, easily tuneable in energy, and narrowly distributed in energy. They thereby offer the means of selectively promoting activated **gas**-surface reactions. The authors report the use of 10% NH3 in He seeded beams to grow GaN and AlN epitaxially on 6H-SiC(0001) and to grow GaN on AlN **buffer layers** deposited on SiC(0001). The III-N films were grown under a variety of incident energies and angles of the NH3 beam, with the III **metal** species supplied from an effusive evaporator source. Film thickness and morphol. were characterized ex situ with Rutherford backscattering spectroscopy, Auger spectroscopy, TEM, and at. force microscopy. Of particular relevance to the III-N growth are the following results: (1) selected energy **epitaxial growth** was obsd., evidently via a direct reaction channel over a barrier of 0.25 .+-. 0.1 eV. A

comparison of films grown at 0.degree. (normal) and 30.degree. angles of NH3 incidence indicated total energy scaling of this chemisorption process. (2) A low energy reaction channel (<0.10 eV) was explicitly confirmed. The mechanism by which this might occur is discussed.
RE.CNT 35 THERE ARE 35 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 42 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:296288 HCAPLUS
DN 130:319145
TI High-quality InGaN films grown by hot-wall epitaxy with mixed (**Ga** + In) source
AU Chu, Shucheng; Saisho, Tetsuhiro; Fujimura, Kazuo; Sakakibara, Shingo; Tanoue, Fumiyasu; Ishino, Kenei; Ishida, Akihiro; Harima, Hiroshi; Chen, Yefan; Yao, Takafumi; Fujiyasu, Hiroshi
CS Miyakoda Technical Center, Suzuki Corporation, Hamamatsu, 431-2103, Japan
SO Japanese Journal of Applied Physics, Part 2: Letters (1999), 38(4B), L427-L428
CODEN: JAPLD8; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB A simple mixed source (**gallium** and In **metals**) method was used in a hot-wall epitaxial system to grow InGaN films on sapphire with thick (.apprx. 1.5 .mu.m) and thin (.apprx. 3 nm) GaN **buffer layers**. **Indium** incorporation was controlled independently by the substrate temp., the N2 partial pressure and the mixed source temp. High-quality InGaN films were obtained, showing strong near-band-edge emission peaks ranging from 370 - 465 nm and narrow x-ray rocking curve full-width at half max. for InGaN of 7.03 arcmin. Nonresonant Raman shift of InGaN layers was clearly obsd. for the 1st time.
IT **25617-97-4**, **Gallium nitride** (GaN)
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(high-quality InGaN films grown by hot-wall epitaxy on sapphire with GaN **buffer layers**)
IT **7440-55-3**, **Gallium**, processes **7440-74-6**, **Indium**, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(high-quality InGaN films grown by hot-wall epitaxy with mixed (**Ga** + In) source)

L44 ANSWER 43 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:266365 HCAPLUS
DN 131:94168
TI Molecular beam **epitaxy growth** of nitride materials
AU Grandjean, N.; Massies, J.
CS Centre de Recherche sur l'Hetero-Epitaxie et ses Applications, Centre National de la Recherche Scientifique, Valbonne, 06560, Fr.
SO Materials Science & Engineering, B: Solid-State Materials for Advanced Technology (1999), B59(1-3), 39-46
CODEN: MSBTEK; ISSN: 0921-5107
PB Elsevier Science S.A.
DT Journal
LA English
AB NH3 was used as a N precursor for growing III-V nitride materials by MBE on c-plane sapphire substrates. The sapphire nitridation step is followed in situ by RHEED. Subsequently, the **buffer layer** growth temp. has a drastic effect on the structural and optical properties of GaN epilayers. The influence of the V/III ratio on the GaN growth is also studied. N-rich conditions lead to the best material properties.

P-type doping is achieved allowing the realization of both GaN and InGaN/GaN based light emitting diodes. The influence of the growth conditions on the properties of InGaN alloys is discussed. The window for optimum growth parameters is very sharp. Finally, AlGaN/GaN quantum wells with a thickness control at the monolayer scale are realized. The smoothness of the interfaces are demonstrated by the linewidth of the QW photoluminescence peak which can be .gtoreq.15 meV. A strong piezoelec. field in the quantum structure is evidenced.

IT **25617-97-4**, Gallium nitride
RL: DEV (Device component use); USES (Uses)
(mol. beam **epitaxy growth** of nitride materials)

IT **24304-00-5**, Aluminum nitride
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PRP (Properties); PROC (Process); USES (Uses)
(mol. beam **epitaxy growth** of nitride materials)

IT **7440-55-3**, Gallium, processes
RL: PEP (Physical, engineering or chemical process); RCT (Reactant); PROC (Process); RACT (Reactant or reagent)
(mol. beam **epitaxy growth** of nitride materials)

RE.CNT 25 THERE ARE 25 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 44 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:113471 HCAPLUS
DN 130:203203
TI Group III nitride semiconductor thin films and manufacture thereof
IN Ohi, Akihiko; Suzuki, Takeshi; Matsui, Toshiyuki; Matsuyama, Hideaki; Kamijo, Hiroshi
PA Fuji Electric Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 11046045	A2	19990216	JP 1997-214070	19970724
PRAI JP 1997-214070		19970724		

AB The manufg. process for forming the nitride thin film on a Si substrate comprises the steps of: forming a hydrogen-end layer by dipping the substrate into an HF soln. or forming a thin **metal layer** on the substrate; forming an optional **buffer layer**; and forming an AlGaInN layer.

IT **7429-90-5**, Aluminum, uses **7440-55-3**, Gallium, uses **24304-00-5**, Aluminum nitride (AlN) **25617-97-4**, Gallium nitride (GaN)
RL: DEV (Device component use); USES (Uses)
(group III nitride semiconductor thin films and manuf. thereof)

L44 ANSWER 45 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:22243 HCAPLUS
DN 130:173437
TI Time of flight mass spectroscopy of recoiled ions studies of surface kinetics and growth peculiarities during gas source molecular beam epitaxy of GaN
AU Kim, Esther; Berishev, I.; Bensaoula, A.; Rusakova, I.; Waters, K.; Schultz, J. A.
CS Space Vacuum Epitaxy Center, University of Houston, Houston, TX, 77204-5507, USA
SO Journal of Applied Physics (1999), 85(2), 1178-1185
CODEN: JAPIAU; ISSN: 0021-8979

PB American Institute of Physics
DT Journal
LA English
AB High growth rate GaN thin films were successfully grown by gas source mol. beam epitaxy and studied in situ by time of flight mass spectroscopy of recoiled ions (TOF-MSRI) and RHEED. We show that TOF-MSRI allows for in situ monitoring and control of sapphire surface chem. and its nitridation. In the latter case, TOF-MSRI is more sensitive to the surface changes during nitridation than RHEED. Using both RHEED and TOF-MSRI, growth of low-temp. GaN **buffer layers** was monitored, and their recrystn. and island-like nature were demonstrated. A model describing the probable growth mechanism for gas source mol. beam epitaxy of GaN is suggested. The model explains both the chem. dissocn. of ammonia at low temp. and the origin of Ga to N TOF-MSRI peak ratio changes for various Ga and ammonia fluxes. High-resoln. transmission electron microscopy studies confirm that GaN films grown with a **buffer layer** have excellent structural quality without any evidence of interfacial defects. Those without a **buffer layer** are highly defective.
IT **25617-97-4P**, Gallium nitride
RL: PEP (Physical, engineering or chemical process); PNU (Preparation, unclassified); PREP (Preparation); PROC (Process)
(time of flight mass spectroscopy of recoiled ions studies of surface kinetics and growth peculiarities during gas source mol. beam epitaxy of GaN)
IT **7440-55-3**, Gallium, reactions
RL: RCT (Reactant); RACT (Reactant or reagent)
(time of flight mass spectroscopy of recoiled ions studies of surface kinetics and growth peculiarities during gas source mol. beam epitaxy of GaN)
RE.CNT 21 THERE ARE 21 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 46 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:793971 HCAPLUS
DN 130:69413
TI Formability and corrosion properties of metal/ceramic multilayer coated strip steels
AU Soderlund, E.; Ljunggren, P.
CS Swedish Institute for Metals Research, Drottning Kristinas vag, Stockholm, S-114 28, Swed.
SO Surface and Coatings Technology (1998), 110(1-2), 94-104
CODEN: SCTEEJ; ISSN: 0257-8972
PB Elsevier Science S.A.
DT Journal
LA English
AB Recently, phys. vapor deposition (PVD) coated strip steel has received growing attention. This work concerns the use of alternating ceramic and **metallic coatings** deposited by PVD to improve simultaneously the formability and corrosion properties of stainless and low carbon strip steels. The coatings were deposited by magnetron sputtering and alternatively electron-beam evapn. In this study, the formability is characterized in terms of the area fraction cracks formed in the coating at strain levels of 5% and 20%, resp. The results show that the crack d. and crack patterns are affected by the substrate strength and topog. as well as by the coating ductility and thickness. A single layer titanium coating showed the lowest crack d., whereas, among a no. of multilayer nitrides, the 3 x (Al/AlN) multilayer coating performed the best. Unlubricated ball-on-flat tests revealed that the friction of a steel ball against the stainless material was significantly lowered with a thin Si coating, whereas none of the surface coatings on the low carbon steel led to decreased friction. The use of a ceramic ball resulted in

lowered friction for many of the nitride coatings compared with the bare low carbon steel substrate. Potentiodynamic measurements show that the coated materials lack the active peak that is typical for the austenitic stainless substrate, which results in a 10- to 50-fold decrease in crit. c.d. compared with the bare substrate. Most of the coatings on stainless steel result in increased resistance to general corrosion even after 20% plastic deformation. Similarly, the undeformed coatings on the low carbon steel showed 3 to 10 times lower corrosion c.d. compared with the substrate. After deformation, as the crack d. increased over approx. 1%, the c.d. also increased. However, Ti and Ti/TiN still provide substantial protection of the mild steel substrate. In this respect, the metallic Ti coating clearly showed a superior behavior to the multilayer coatings, including the Ti/TiN coatings.

IT **7429-90-5**, Aluminum, properties **24304-00-5**, Aluminum nitride aln
RL: PRP (Properties); TEM (Technical or engineered material use); USES (Uses)
(multilayer coatings; formability and corrosion resistance of **metal/nitride** ceramic multilayer coated strip steels)

RE.CNT 19 THERE ARE 19 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 47 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:774818 HCAPLUS
DN 130:59732
TI Study of the growth of thin Mg films on wurtzite GaN surfaces
AU Bermudez, V. M.
CS Naval Research Laboratory, Washington, DC, 20375-5347, USA
SO Surface Science (1998), 417(1), 30-40
CODEN: SUSCAS; ISSN: 0039-6028
PB Elsevier Science B.V.
DT Journal
LA English
AB The growth, structure and electronic properties of thin (.ltoreq.20 .ANG. thick) Mg films on clean, n-type wurtzite GaN have been studied using Auger, photoemission and electron-energy-loss spectroscopies and LEED. **Epitaxial growth** occurs near 300 K leading to a (1 .times. 1)-ordered **metal layer**. Site exchange between Mg and Ga releases free Ga, which remains near the interface, and incorporates Mg into the GaN near the interface. Deposition of less than one monolayer of Mg moves the Fermi level .apprx.0.60 eV farther down into the gap, from the initial position of 2.60 eV above the valence band max., where it remains essentially fixed with increasing Mg coverage. Annealing leads to desorption of metallic Mg which, for a thin film, is essentially complete at .apprx.520 K. There is no indication of extensive intermixing of either Ga or N with the Mg. A residue of Ga and Mg adatoms or small non-metallic clusters, remaining after desorption of the metal, persists to at least 620 K. Desorption of metallic Mg has little or no effect on the Fermi-level position which, therefore, is detd. mainly by trapping of electrons by acceptors that result from Mg incorporation into the surface, rather than by Schottky-barrier formation.

IT **7440-55-3**, Gallium, properties
RL: PRP (Properties); REM (Removal or disposal); PROC (Process)
(releasing from gallium nitride substrate; growth of thin Mg films on wurtzite GaN surfaces)

IT **25617-97-4**, Gallium nitride (GaN)
RL: DEV (Device component use); PRP (Properties); USES (Uses)
(substrate; growth of thin Mg films on wurtzite GaN surfaces)

RE.CNT 54 THERE ARE 54 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 48 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:618778 HCAPLUS
DN 129:252751
TI Epitaxial wafer having a gallium nitride epitaxial layer deposited on semiconductor substrate and method for preparing it
IN Motoki, Kensaku; Matsushima, Masato; Akita, Katsushi; Shimazu, Mitsuru; Takemoto, Kikurou; Seki, Hisashi; Koukitu, Akinori
PA Sumitomo Electric Industries, Ltd., Japan
SO Eur. Pat. Appl., 11 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 865088	A2	19980916	EP 1998-301948	19980316
	EP 865088	A3	20000823		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 10316498	A2	19981202	JP 1998-78333	19980311
	US 6270587	B1	20010807	US 1998-41109	19980312
	CN 1197998	A	19981104	CN 1998-109431	19980313
	US 6387722	B1	20020514	US 2000-578704	20000526
PRAI	JP 1997-82319	A	19970314		
	JP 1998-78333	A	19980311		
	US 1998-41109	A3	19980312		

AB The present invention provides an epitaxial wafer comprising a (111) substrate of a semiconductor having cubic crystal structure, a 1st GaN layer having a thickness of 60 nm or more, a 2nd GaN layer having a thickness of 0.1 .mu.m or more and a method for prepg. it. The epitaxial GaN layers can be grown on a GaAs (111) substrate.
IT **25617-97-4**, Gallium nitride
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(growth of **buffer** and epitaxial layers of gallium nitride on semiconductor substrate)
IT **7440-55-3**, Gallium, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(in growth of **buffer** and epitaxial layers of gallium nitride on gallium arsenide substrate)

L44 ANSWER 49 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:175669 HCAPLUS
DN 128:263701
TI Nitride semiconductor laser elements
IN Aneo, Masayuki; Nakamura, Shuji
PA Nichia Chemical Industries Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10075008	A2	19980317	JP 1996-229161	19960830
PRAI	JP 1996-229161		19960830		

AB The elements comprise: a sapphire or a MgAl2O4 substrate; a GaN **buffer layer**; an n-GaN layer contacting with a Ti/Al n-electrode; an n-In0.1Ga0.9N crack-preventing layer; an n-Al0.2Ga0.8N light-confinement layer; an n-GaN light-guide layer; an In0.2Ga0.8N-well/In0.05Ga0.95N-barrier MQW active layer; a p-Al0.1Ga0.9N cap layer; a p-GaN light-guide layer; a p-Al0.2Ga0.8N light-confinement

layer; a p-GaN contact layer; and a Ni/Au p electrode.
IT **7429-90-5**, Aluminum, uses **25617-97-4**, Gallium nitride (GaN)
RL: DEV (Device component use); USES (Uses)
(nitride semiconductor laser elements)

L44 ANSWER 50 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:791380 HCAPLUS
DN 128:78679
TI New buffering process in preparation of high quality GaN films
AU Hwang, Jin Soo; Seong, Seeyearl; Tanaka, Satoru; Iwai, Sohachi; Aoyagi, Yoshinobu; Chong, Paul Joe
CS Korea Research Institute of Chemical Technology, Taejon, 305-606, S. Korea
SO Bulletin of the Korean Chemical Society (1997), 18(11), 1133-1135
CODEN: BKCSDE; ISSN: 0253-2964
PB Korean Chemical Society
DT Journal
LA English
AB A buffering process in the prepn. of GaN films on AlN **buffer layer**/6H-SiC substrate systems is described. The growth system was a conventional **metal** org. CVD (MOCVD). In the conventional MOCVD process, the gaseous trimethylgallium (TMG) and NH3 are carried into a reactor sep. and then mixed at the reaction zone. The new process has been carried out by the alternating pulsative supply (APS) of reactant gases TMG, NH3 and purging **gas** H2 for 5 cycles on the AlN **buffer layers**. The APS is a pretreatment process preformed on the **buffer layers** before the normal MOCVD process to improve the quality of GaN films. The Si faces of 6H-SiC substrate were used for the **epitaxial growth** of GaN. The substrate surface was etched conventionally. A graphite susceptor coated with SiC was heated by rf induction. The growth temp. was 1060.degree.. The AlN **buffer layers** were prepd. using 2.4 .mu.mol/min trimethylaluminum (TMAl) and 2 slm ammonia. The TMAl was delivered into the reactor with H2 **gas**. After deposition of AlN buffers, the initial layers were made by the following process: serial injection of 32 .mu.mol/min of TMG carried by H2, followed by purging the system with H2. The 2 slm ammonia was supplied, followed by H2 purge. Each **gas** was alternately supplied into the reactor for every 1 s. The whole cycle of reactants supply was repeated 5 times. Then the main GaN films were grown on wetted GaN layers using 32 .mu.mol/min TMG with carrier H2, 2 slm ammonia and 0.5 slm N2 for 20 min. The growth rate of the GaN films, estd. by high-resoln. SEM for lateral view, was about 300 .ANG./min. The films fabricated by this process demonstrated very low defect d.
RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 51 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:656928 HCAPLUS
DN 127:287231
TI Bisamido azides of **gallium**, **aluminum** and **indium** and their use as precursors for the growth of nitride films
IN Neumayer, Deborah Ann; Lakhotia, Vikas
PA University of Texas System, USA
SO U.S., 5 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI US 5675028 A 19971007 US 1995-520680 19950829
PRAI US 1995-520680 19950829
OS MARPAT 127:287231
AB Disclosed are bisamido azides of **Ga**, **Al**, or In which when pyrolyzed in accordance with the invention, produce **metal nitride** films on a substrate. Included are bisamido azides [(RR'N)2M(N3)]n (R, R' = H, alkyl, alkylamine, aryl, alkyl-substituted aryl, alkylsilyl, halo, or together for a cycloalkyl; M = **Ga**, **Al**, In; n = 1 to about 6). Examples are given for the synthesis of [(Me2N)2GaN3]2 (1, characterized by x-ray crystallog.), [(RR'N)2GaN3]2 (RR'N = 2,2,6,6-tetramethylpiperidino), and [{(Me2N)CH2CH2NEt}2GaN3]. Amorphous film growth of GaN was achieved as low as 250.degree. on (0001) sapphire with bis(dimethylamido)**gallium** azide 1 as MOCVD precursor. Higher temps. achieved **epitaxial growth**. **Epitaxial growth** of GaN was also achieved on (100) GaAs substrate at 500.degree.. The bisamido azides provide a safer precursor for nitride film growth than other more pyrophoric, potentially explosive alternatives, which results in storage cost-savings and better ease in handling. Facile elimination of the amido ligands results in significant redn. in carbon incorporation in the films and a substantial redn. in growth temp. The **metal nitride** films made from these bisamido azides may be useful in a range of applications in the electronics industry.
IT **7429-90-5DP**, **Aluminum**, bisamido azide complexes, preparation **7440-55-3DP**, **Gallium**, bisamido azide complexes, preparation **7440-74-6DP**, **Indium**, bisamido azide complexes, preparation
RL: RCT (Reactant); SPN (Synthetic preparation); PREP (Preparation); RACT (Reactant or reagent)
(prepn. as precursors for MOCVD growth of nitride films)
IT **25617-97-4P**, **Gallium nitride** (GaN)
RL: SPN (Synthetic preparation); PREP (Preparation)
(prepn. of **gallium nitride** films on (0001) sapphire and (100) GaAs substrates by MOCVD of **gallium** bisamido azide)

L44 ANSWER 52 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:579851 HCAPLUS
DN 127:255619
TI Method of **epitaxial growth** of monocrystalline Group IIIA **metal nitrides**
IN Vodakov, Jury Alexandrovich; Mokhov, Evgeny Nikolaevich; Ramm, Mark Grigorievich; Roenkov, Alexandr Dmitrievich; Makarov, Jury Nikolaevich; Karpov, Sergei Jurievich; Ramm, Mark Spiridonovich
PA Vodakov, Jury Alexandrovich, Russia; Mokhov, Evgeny Nikolaevich; Ramm, Mark Grigorievich; Roenkov, Alexandr Dmitrievich; Makarov, Jury Nikolaevich; Karpov, Sergei Jurievich; Ramm, Mark Spiridonovich
SO PCT Int. Appl., 17 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9731140	A1	19970828	WO 1997-RU31	19970211
	W: CA, CN, JP, KR, US				
	RW: AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	RU 2097452	C1	19971127	RU 1996-103332	19960222
PRAI	RU 1996-103332		19960222		

AB The method of vapor-phase **epitaxial growth** of monocryst. nitride of at least one metal belonging to Group IIIA comprises arrangement in parallel, opposite each other, of the evapg. surface of a

source of the metal specified in the compn. of the single crystal grown and the growing surface of the substrate, defining the growth zone, generation in the growth zone of an NH3 flux, heating of the source and the substrate up to temps. providing the growth of the single crystal on the substrate, while maintaining the temp. of the source above the temp. of the substrate. The material of the source is a mixt. contg. a metallic component including at least one free metal specified in the compn. of the single crystal grown, and a nitride component including at least one nitride of at least one metal specified in the compn. of the single crystal grown. For example, single-crystal GaN was grown by this method.

IT **24304-00-5, Aluminum nitride**
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(VPE of **aluminum gallium nitride** using polycryst. powd.)

IT **25617-98-5, Indium nitride**
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(VPE of **gallium indium nitride** using polycryst. powd.)

IT **7440-55-3, Gallium**, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(VPE of **gallium nitride** and **aluminum gallium nitride** using molten)

IT **25617-97-4, Gallium nitride**
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(method for VPE of)

L44 ANSWER 53 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:391000 HCAPLUS
DN 127:26433
TI Fabrication of a remote plasma-enhanced metalorganic chemical vapor deposition system and low-temperature growth of GaN this films on (0001) sapphire substrates
AU Sone, Cheolsoo; Kim, Min Hong; Yi, Jae-Hyung; Yoon, Euijoon; Heur, Soun Ok
CS School of Materials Science and Engineering, Seoul National University, Seoul, 151-742, S. Korea
SO Ungyong Mulli (1997), 10(2), 133-139
CODEN: HMHMEY; ISSN: 1013-7009
PB Korean Physical Society
DT Journal
LA Korean
AB GaN this films were grown on (0001) sapphire substrates without **buffer layers** by using a remote plasma-enhanced **metal**-org. CVD (RPE-MOCVD)technique using triethylgallium and N2 plasma as reactant sources. The optical emission spectra obtained from the N2 plasma were dominated by the 1st pos. and the 2nd pos. mol. N transitions. The d. of the activated N mols. varied with position, radio-frequency power, reactor pressure, and N flow rate. The effectiveness of the N plasma increased with increasing radio-frequency power, reactor pressure, and N flow rate. The effectiveness of the N plasma increased with increasing radio-frequency power and **gas** flow rate, but with decreasing reactor pressure. The crystallinity and the surface morphol. of the films changed with total pressure, growth temp., radio-frequency power, and V/III ratio. Highly oriented (0001) GaN films were deposited on the (0001) sapphire substrates at relatively low temps., such as 500.degree.. The surface morphol. of the GaN films improved with increasing V/III ratio and radio-frequency power, but the crystallinity deteriorated with increasing radio-frequency power at 500.degree.. The structural properties of the GaN films improved as the growth temp. increased.

L44 ANSWER 54 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:361412 HCAPLUS
DN 126:337633
TI Structural elements comprising a substrate and a nitride semiconductor heterostructure
IN Riechert, Henning; Straus, Uwe
PA Siemens A.-G., Germany
SO Ger., 4 pp.
CODEN: GWXXAW
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 19613265	C1	19970417	DE 1996-19613265	19960402
	EP 800214	A1	19971008	EP 1997-104416	19970314
	R: DE, FR, GB				
	JP 10041230	A2	19980213	JP 1997-96411	19970331
PRAI	DE 1996-19613265		19960402		

AB For radiation generation or charge carrier control, the structural elements comprise an active layer of Group III-V semiconductor material. In this active layer, the Group-III component contains .gtoreq.20% at. In, and the Group-V component contains N. The structural elements comprise a **buffer layer** of Group III-V semiconductor material between the substrate and the active layer. In this **buffer layer**, the Group-III component contains In, and the Group-V component contains N. The compn. of the semiconductor material of the active layer is different from that of the semiconductor material contacting the active layer on the side facing the substrate, causing a change in energy band gap at the interface. The active layer has a lattice const. corresponding to a for **epitaxial growth** typical temp. of the lattice const. of the **buffer layer**. These structural elements can be formed on a conventional substrates or semiconductor material without In content. The substrate or layer on the substrate is selected from GaN, AlGaN, AlN, sapphire, and SiC, and the method is esp. suitable for use as high-electron-mobility transistors and for radiation generation in the blue and green spectrum.
IT **7440-74-6**, Indium, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(active layer and **buffer layer** contg.; structural elements for HEMTs comprising a substrate and)
IT **24304-00-5**, Aluminum nitride **25617-97-4**, Gallium nitride
RL: TEM (Technical or engineered material use); USES (Uses)
(layer; structural elements comprising a substrate and)

L44 ANSWER 55 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:238537 HCAPLUS
DN 126:349771
TI ZnO buffer formed on Si and sapphire substrates for GaN MOVPE
AU Shirasawa, T.; Honda, T.; Koyama, F.; Iga, K.
CS P & I Lab., Tokyo Inst. of Technology, Yokohama, 226, Japan
SO Materials Research Society Symposium Proceedings (1997), 449(III-V Nitrides), 373-377
CODEN: MRSPDH; ISSN: 0272-9172
PB Materials Research Society
DT Journal
LA English
AB ZnO layers were deposited by electron beam (EB) evapn. and laser ablation MBE as **buffer layers** to grow GaN by **metal** org. VPE (OMVPE). The photoluminescence spectrum of the ZnO layer deposited by an EB evaporator shows an emission peaks of 367 nm. GaN was

grown on ZnO/Si, Si and sapphire substrates under the same growth condition employing low-temp.-grown AlN buffers to prevent the dissocn. of ZnO during the high GaN growth. The GaN on ZnO/Si shows sharp photoluminescence spectra at room temp. and 10 K. These results indicate a potential use of ZnO/Si substrates for GaN based blue-UV optical devices such as vertical-cavity surface-emitting lasers (VCSELs).

L44 ANSWER 56 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:190808 HCAPLUS
DN 126:310816
TI Growth of zinc-blende GaN on GaAs (100) substrates at high temperature using low-pressure MOVPE with a low V/III molar ratio
AU Nakadaira, Atsushi; Tanaka, Hidenao
CS NTT Integrated Information & Energy Systems Laboratories, Musashino, 180, Japan
SO Journal of Electronic Materials (1997), 26(3), 320-324
CODEN: JECMA5; ISSN: 0361-5235
PB Minerals, Metals & Materials Society
DT Journal
LA English
AB Zinc-blende GaN films were grown on GaAs (100) substrates by low-pressure **metal**-org. vapor phase epitaxy using trimethylgallium or triethylgallium and NH3. Films grown at lower temps. contained considerable amts. of carbon, but the carbon concn. was reduced in high temp. growth. When the film was grown at 950.degree.C using triethylgallium and NH3, its carbon concn. was on the order of 1017 cm-3. The cryst. and optical quality of zinc-blende GaN crystal also improved with high-temp. growth at a low V/III ratio using a thin **buffer layer**. The films exhibited only one sharp photoluminescence peak at 3.20 eV with a full width at half max. as low as 70 meV at room temp.

L44 ANSWER 57 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:102671 HCAPLUS
DN 126:257649
TI Theoretical model for analysis and optimization of group III-nitrides growth by molecular beam epitaxy
AU Averyanova, M. V.; Karpov, S. Yu.; Makarov, Yu. N.; Przhevalskii, I. N.; Ramm, M. S.; Talalaev, R. A.
CS Russian Res. Cent. "Applied Chem.", St. Petersburg, Russia
SO MRS Internet Journal of Nitride Semiconductor Research [Electronic Publication] (1996), 1, No pp. Given
CODEN: MIJNF7
URL: http://nsr.mij.org/1/31/complete.html
PB Materials Research Society
DT Journal
LA English
AB A theor. model which accounts for a physisorption precursor of mol. nitrogen is proposed for the anal. of group III-nitride growth by mol. beam epitaxy (MBE). The kinetics of nitrogen evapn. are found to be an essential factor influencing the MBE growth process of group III-nitrides. The high thermal stability of nitrides is explained to be related to the desorption kinetics resulting in a low value of the evapn. coeff. The values of the evapn. coeffs. as functions of temp. are extd. from the exptl. Langmuir evapn. data of GaN and AlN. Using the revised thermodn. properties of the group III-nitrides, and the obtained values of the evapn. coeff., the process parameter dependent growth rate and transition to extra liq. phase formation during the GaN MBE are calcd. The theor. results are compared to the available exptl. data.

L44 ANSWER 58 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1996:640332 HCAPLUS

DN 126:38942
TI Vapor phase epitaxy of GaN using gallium tri-chloride and ammonia
AU Yuri, M.; Ueda, T.; Lee, H.; Itoh, K.; Baba, T.; Harris, J. S., Jr.
CS Solid State Electronics Lab., Stanford Univ., Stanford, CA, 94305-4075, USA
SO Materials Research Society Symposium Proceedings (1996), 421(Compound Semiconductor Electronics and Photonics), 195-200
CODEN: MRSPDH; ISSN: 0272-9172
PB Materials Research Society
DT Journal
LA English
AB GaN films with good cryst. quality are grown on sapphire by atm. pressure vapor phase epitaxy using GaCl3 and NH3. **Epitaxial growth** is carried out over temp. and V/III-ratio ranges of 800-1000.degree. and 100-1000, resp. Typical growth rate obtained is at 5-20 .mu.m/h. The films grown <925.degree. typically show three dimensional (island) growth, while above that temp., continuous films were obtained. Films grown at 975.degree. with a V/III ratio > 300 exhibit a smooth surface. XRD anal. shows that the films are single crystal with hexagonal polytype. Strong band-edge photoluminescence is obsd. with a FWHM of 60 meV at room temp. and 25 meV at 77 K. This dimple growth technique is effective for growing high quality bulk GaN, which can be used as a substrate for subsequent epitaxy. To further improve the surface morphol., a preliminary expt. with GaN growth on a thin GaN **buffer layer** prepd. by gas source MBE is also presented.
IT **7440-55-3**, Gallium, reactions
RL: RCT (Reactant); RACT (Reactant or reagent)
(gas source MBE of GaN **buffer layer** using)
IT **25617-97-4P**, Gallium nitride (GaN)
RL: PEP (Physical, engineering or chemical process); PRP (Properties); SPN (Synthetic preparation); PREP (Preparation); PROC (Process)
(photoluminescence of VPE-grown GaN using GaCl3 and NH3)

L44 ANSWER 59 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1996:431672 HCAPLUS
DN 125:102747
TI Manufacture of laminated ceramic capacitors
IN Kubodera, Noryuki; Kono, Yoshiaki
PA Murata Manufacturing Co, Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08124789	A2	19960517	JP 1994-256739	19941021
PRAI	JP 1994-256739		19941021		

AB **Metal films** are laminated into single bodies, sintered, and partially nitrogenated to form **metal nitride** ceramics (e.g., AlN).
IT **7429-90-5**, Aluminum, uses
RL: DEV (Device component use); RCT (Reactant); RACT (Reactant or reagent); USES (Uses)
(metal nitrogenation in manuf. of laminated ceramic capacitors)
IT **24304-00-5P**, Aluminum nitride
RL: DEV (Device component use); PNU (Preparation, unclassified); PREP (Preparation); USES (Uses)
(metal nitrogenation in manuf. of laminated ceramic capacitors contg.)

L44 ANSWER 60 OF 67 HCAPLUS COPYRIGHT 2003 ACS

03/21/2003

AN 1996:87892 HCAPLUS
DN 124:303246
TI Crystal growth of **gallium nitride**-base compound semiconductor by metalorganic vapor deposition
IN Nakamura, Shuji
PA Nichia Kagaku Kogyo Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07312350	A2	19951128	JP 1995-152676	19950525
	JP 3257344	B2	20020218		
	JP 2002154900	A2	20020528	JP 2001-266561	19910327
PRAI	JP 1995-152676	A3	19950525		

AB The title method involves growing a GaxAl1-xN (x = 0.5-1) **buffer layer** at 200-900.degree. and growing a GaN-base compd. semiconductor crystal on the **buffer layer** by org. **metal** vapor deposition. The obtained semiconductor crystal showed improved crystallinity.

L44 ANSWER 61 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1994:20350 HCAPLUS
DN 120:20350
TI Reversible changes in doping of **indium gallium aluminum nitride** alloys induced by ion implantation or hydrogenation
AU Pearton, S. J.; Abernathy, C. R.; Wisk, P. W.; Hobson, W. S.; Ren, F.
CS AT and T Bell Lab., Murray Hill, NJ, 07974, USA
SO Applied Physics Letters (1993), 63(8), 1143-5
CODEN: APPLAB; ISSN: 0003-6951
DT Journal
LA English
AB Carrier concns. in doped InN, In0.37Ga0.63N, and In0.75Al0.25N layers are reduced by both F+ ion implantation to produce resistive material for device isolation, and by exposure to a hydrogen plasma. In the former case, post-implant annealing at 450-500.degree. produces sheet resistances >106 .OMEGA./.box. in initially n+ (7 .times. 1018-3 .times. 1019 cm-3) ternary layers and values of .apprx.5 .times. 103 .OMEGA./.box. in initially degenerately doped (4 .times. 1020 cm-3) InN. The evolution of sheet resistance with post-implant annealing temp. is consistent with the introduction of deep acceptor states by the ion bombardment, and the subsequent removal of these states at temps. .ltorsim.500.degree. where the initial carrier concns. are restored. Hydrogenation of the nitrides at 200.degree. reduces the n-type doping levels by 1-2 orders of magnitude and suggests that unintentional carrier passivation occurring during cool down after **epitaxial growth** may play a role in detg. the apparent doping efficiency in these materials.

L44 ANSWER 62 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1992:494810 HCAPLUS
DN 117:94810
TI Spray coating of metal strips with molten metal and powder
IN Yamaguchi, Susumu; Miki, Toshihiko; Uchida, Hiroyuki; Onaka, Itsuo
PA Shinnippon Seitetsu K. K., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese

FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 04052263	A2	19920220	JP 1990-164729	19900621
PRAI JP 1990-164729		19900621		

AB The process, useful for coating of metal strips (e.g., Fe, Cu, Al), esp. steel strips, with powder-dispersed **metal layers** (e.g., Zn), comprises dispersing the powder in the molten metal before, during or after spraying of the molten metal. The powder, having particle size .ltoreq.50% of the coating thickness, is metal (e.g., Al), metal oxide (e.g., Al2O3), **metal nitride** (e.g., TiN), metal carbide (e.g., SiC) and/or metal boride (e.g., Cr3B2). The **metal coating** layer contains the powder .gtoreq.0.1 mg/m2.

IT **7429-90-5**, Aluminum, uses **10043-11-5**, Boron nitride (BN), uses
RL: USES (Uses)
(powder, metal contg., coating with, of metal strips, by melt-spray)

IT **7429-90-5**, Aluminum, uses
RL: USES (Uses)
(powder, zinc contg., coating with, of steel strips, by melt-spray)

L44 ANSWER 63 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1992:73180 HCAPLUS
DN 116:73180
TI Manufacture of film by irradiating ion beam
IN Ogata, Kiyoshi; Ando, Yasunori
PA Nissin Electric Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese

FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 03202468	A2	19910904	JP 1989-342778	19891229
JP 2844779	B2	19990106		
PRAI JP 1989-342778		19891229		

AB The film is manufd. by irradiating a substrate with a metal ion beam and a vapor ion beam simultaneously or alternatively. A metal, metal oxide, or **metal nitride** film is obtained by using an inert gas, O, or N ion beam. An AlN film on an Al2O3 ceramic was obtained by using an Al ion beam and a N ion beam.

IT **7429-90-5**, Aluminum, uses
RL: USES (Uses)
(ion beam, for manuf. of aluminum nitride film)

IT **24304-00-5P**, Aluminum nitride
RL: SPN (Synthetic preparation); PREP (Preparation)
(prepn. of film of, by irradn. with aluminum ion beam and nitrogen ion beam)

L44 ANSWER 64 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1987:627372 HCAPLUS
DN 107:227372
TI An intrinsic stress scaling law for polycrystalline thin films prepared by ion beam sputtering
AU Windischmann, H.
CS Stand. Oil Co., Cleveland, OH, 44128, USA
SO Journal of Applied Physics (1987), 62(5), 1800-7
CODEN: JAPIAU; ISSN: 0021-8979
DT Journal
LA English

AB The intrinsic stresses of Al, Ti, Fe, Ta, Mo, W, Ge, Si, AlN, TiN, and Si3N4 films prepd. by ion beam sputtering were investigated at low Td/Tm values, where Td and Tm are the abs. deposition temp. and melting temp., resp. The intrinsic stress is compressive, and its origin is explained in terms of the ion peening model. The intrinsic stress is compressive, and its origin is explained in terms of the ion peening model. The Knock-on linear cascade theory of forward sputtering is applied to derive a simple scaling law with the film's phys. properties. The stress is directly proportional to the elastic energy/mol, given by the quantity Q = EM/(1 - .nu.)D, where E is Young's modulus, M the at. mass, D the d., and .nu. Poisson's ratio. Stress data taken from the literature for a variety of materials deposited by low-pressure magnetron sputtering, and radio-frequency and ion beam sputtering also fit the correlation with Q. Further, the model predicts a square-root dependent on the incident ion energy, suggesting that the stress is momentum rather than energy driven.

IT **7429-90-5**, Aluminum, properties **24304-00-5**, Silicon
RL: PRP (Properties)
(ion beam sputtering and intrinsic stress of)

L44 ANSWER 65 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1986:525518 HCAPLUS
DN 105:125518
TI Semiconductor device comprising a Schottky contact
IN Marengo, Michel; Kohn, Erhard; Cathelin, Michel
PA Thomson-CSF S. A., Fr.
SO Fr. Demande, 13 pp.
CODEN: FRXXBL
DT Patent
LA French
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	FR 2571548	A1	19860411	FR 1984-15491	19841009
	FR 2571548	B1	19870724		
PRAI	FR 1984-15491		19841009		

AB A semiconductor device comprises a Schottky contact, with improved annealing characteristics, which is formed between a refractory **metal layer** and a semiconductor layer; an interfacial layer, which serves as a diffusion barrier, is formed between the refractory **metal layer** and the semiconductor layer. The interfacial layer is preferably a **metal nitride** and has a thickness of tens of .ANG.. The refractory **metal layer** is selected from W, Ti, Al, Ta, and Si and the diffusion barrier is selected from WSiN, TiWSiN and WAlN. The semiconductor material is chosen from Si and Group IIIA pnictides such as GaAs, AlGaAs and InP. The Schottky contact is used in a metal-semiconductor FET and a varactor.

IT **7429-90-5**, uses and miscellaneous
RL: USES (Uses)
(Schottky contact contg. layer from)

IT **24304-00-5D**, solid solns. with refractory **metal nitrides** and silicides
RL: USES (Uses)
(diffusion barrier from layer of, in Schottky contacts)

L44 ANSWER 66 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1986:43704 HCAPLUS
DN 104:43704
TI Growing compound semiconductor thin films
IN Maebotoke, Sakae; Kobayashi, Morio
PA Nippon Telegraph and Telephone Public Corp., Japan

SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 60173829	A2	19850907	JP 1984-24444	19840214
JP 05086646	B4	19931213		
PRAI JP 1984-24444		19840214		

AB An a.c. bias voltage is applied between a target consisting of >1 of Al, Ga, and In and a conductive substrate having a metal evapn. coating on sapphire (C plane) or optically abraded glass to form an AlxGa1-xN (0 .ltoreq. x .ltoreq. 1) layer or InN **buffer layer** by high frequency sputtering in N; the treated substrate is then placed in a low pressure vessel, heated in a NH3-contg. atm. along with a Group IIIA organometallic compd. to form a film of the same nitride as the **buffer layer** by epitaxial vapor deposition. Epitaxial films having few N lattice voids are manufd. Thus, a.c. bias voltage was applied between an optically abraded sapphire (C plane) and a Ga metal target in an atm. of Ar and N to form a 1000-7000 .ANG. thick GaN **buffer layer**. The treated substrate was placed in a low pressure atm. contg. Me3Ga, NH3, and N, and heated to form 1-10 .mu. thick C-axis-oriented GaN epitaxial layer having a carrier concn. of 108 cm-3 and resistivity 10-1 .OMEGA.-cm. The resulting film showed a greater luminescence, indicating a decline in the no. of non-luminescing centers and therefore better crystallinity, than a film without the **buffer layer**.

IT **24304-00-5D**, solid solns. with gallium nitride **25617-97-4D**, solid solns. with aluminum nitride **25617-98-5**
RL: PROC (Process)
(epitaxy of, **buffer layer** for, on **metal-coated** substrates)

IT **7429-90-5**, uses and miscellaneous **7440-55-3**, uses and miscellaneous **7440-74-6**, uses and miscellaneous
RL: USES (Uses)
(sputtering of, for **buffer layer** for Group IIIA element nitride epitaxy)

L44 ANSWER 67 OF 67 HCAPLUS COPYRIGHT 2003 ACS
AN 1976:24808 HCAPLUS
DN 84:24808
TI Growth of **metal nitride** single crystals
IN Minakawa, Shigekazu; Shintani, Akira; Saito, Tadashi
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 50079500	A2	19750627	JP 1973-129260	19731119
PRAI JP 1973-129260		19731119		

AB A **metal nitride** crystal is **epitaxially grown** on an acid-sol. metal oxide seed crystal whose lattice consts. are similar to those of the nitride crystal, and the metal oxide seed crystal is dissolved in an acid to give a **metal nitride** single-crystal plate. The nitride crystal plate is used as a seed crystal for the vapor-phase **epitaxial growth** of another (or the same) **metal nitride** crystal by

using the reaction of a metal halide with NH3, and optionally, acceptor-forming dopants such as Zn, Be, Mg, and Cd may be added during the initial or intermediate stages of the **gas**-phase **epitaxial growth** of the 2nd nitride crystal to give a **metal nitride** crystal having i-n junction. The method yields **metal nitride** (such as GaN) crystals having very little defects, and hence, the method is useful for the prepn. of semiconductive **metal nitride** crystals. Thus, H 10 ml/min was passed through a bubbler contg. GaMe3 (0.degree.) and led into a crystal growing app. contg. a ZnO seed crystal [(0001) plane as the crystal growing surface] heated at 900.degree., while a mixt. of NH3 500 and H 4000 ml/min was also fed into the crystal growing app. to grow a GaN sngle crystal (3 .mu./hr); the crystal contained C as impurity and had a yellowish color. Then the ZnO seed crystal was removed by dissoln. in acid, and the GaN crystal was heated (1030.degree.) in a crystal growing app. contg. a **Ga** source (950.degree.), and high-purity HCl 5 ml/min was introduced over the **Ga** source while a NH3 500-Ar 2000 ml/min mixt. was fed into the tube from the other end to give a colorless n-type GaN crystal (2 .mu./hr); the no. of etch pits obsd. (200.degree. H3PO4 etching) was 104/cm2.

L68 ANSWER 1 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 2003-151174 [15] WPIX
DNN N2003-119352 DNC C2003-039442
TI Growth of **gallium nitride** epitaxial layer for electronic devices, involves growing **gallium nitride buffer layer** on substrate, raising temperature of substrate and growing **gallium nitride** epitaxial layer.
DC E32 L03 U11 U12
PA (SUME) SUMITOMO ELECTRIC IND CO
CYC 1
PI JP 2002293697 A 20021009 (200315)* 6p
ADT JP 2002293697 A JP 2001-96203 20010329
PRAI JP 2001-96203 20010329
AB JP2002293697 A UPAB: 20030303
NOVELTY - A **gallium nitride buffer layer** (20) is formed on a **gallium**-arsenic substrate (10). The temperature of the substrate is raised in less than 35 minutes to a temperature for **epitaxial growth** from the temperature at which layer (20) is formed, and a **gallium nitride** epitaxial layer (30) is formed on **buffer layer**.
USE - For growing **gallium nitride** epitaxial layer for bluish violet color laser, light emitting diode and high frequency-high output electronic device.
ADVANTAGE - **Gallium nitride** epitaxial layer having favorable crystal quality is grown on a substrate in a shorter duration.
DESCRIPTION OF DRAWING(S) - The figure shows the growth of **gallium nitride** epitaxial layer. (Drawing includes non-English language text).
Substrate 10
Buffer layer 20
Epitaxial layer 30
Dwg.1/5

L68 ANSWER 2 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 2003-061738 [06] WPIX
DNN N2003-047626 DNC C2003-016489
TI Semiconductor thin film formation method e.g. for **gallium nitride** thin film for blue semiconductor light-emission device, involves converting polarity of **gallium nitride** layer from negative to positive on **epitaxial growth** surface.
DC L03 U11 U12
PA (FUTK) FUTABA DENSHI KOGYO KK; (YOSH-I) YOSHIKAWA A
CYC 1
PI JP 2002270525 A 20020920 (200306)* 7p
ADT JP 2002270525 A JP 2001-71746 20010314
PRAI JP 2001-71746 20010314
AB JP2002270525 A UPAB: 20030124
NOVELTY - **Aluminum** monolayer and **gallium nitride buffer layers** are formed on sapphire substrate such that **buffer layer** has polycrystalline structure, and priority orientation of **aluminum** is performed with respect to single crystal. **Epitaxial growth** of **gallium nitride** layer is performed on substrate such that polarity of **gallium nitride** layer changes from negative to positive on **epitaxial growth** surface.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(1) semiconductor thin film;

(2) semiconductor device; and
(3) substrate.
USE - For forming semiconductor thin film (claimed) such as **gallium nitride** (GaN) thin film for blue semiconductor light-emission device, blue semiconductor laser.
ADVANTAGE - Since the polarity on the semiconductor surface is converted into positive, the optical characteristics are improved.
DESCRIPTION OF DRAWING(S) - The figure shows the model of **gallium** surface of GaN structure comprising **aluminum** monolayer.
Dwg.4/4

L68 ANSWER 3 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 2002-668694 [72] WPIX
DNN N2002-529051 DNC C2002-187989
TI Production process for GaN crystal substrate for laser diodes, comprises depositing **metal film** on starting substrate, depositing **gallium nitride** film to form laminate substrate, and removing starting substrate from laminate substrate.
DC L03 U11 U12
IN KURODA, N; SHIBATA, M
PA (HITD) HITACHI CABLE CO LTD; (HITD) HITACHI CABLE LTD; (NIDE) NEC CORP; (KURO-I) KURODA N; (SHIB-I) SHIBATA M
CYC 30
PI EP 1245702 A2 20021002 (200272)* EN 17p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
JP 2002284600 A 20021003 (200280) 12p
US 2002175340 A1 20021128 (200281)
KR 2002076167 A 20021009 (200314)
CN 1378238 A 20021106 (200316)
ADT EP 1245702 A2 EP 2002-252184 20020326; JP 2002284600 A JP 2001-88294 20010326; US 2002175340 A1 US 2002-106693 20020326; KR 2002076167 A KR 2002-16387 20020326; CN 1378238 A CN 2002-107886 20020326
PRAI JP 2001-88294 20010326
AB EP 1245702 A UPAB: 20021108
NOVELTY - Process for producing a **gallium nitride** crystal substrate comprises: depositing a **metal film** on a starting substrate; depositing a **gallium nitride** film on the **metal film** to form a laminate substrate; and removing the starting substrate from the laminate substrate on which the **gallium nitride** film is deposited to form a free standing **gallium nitride** crystal substrate.
DETAILED DESCRIPTION - Process for producing a **gallium nitride** crystal substrate comprises:
(a) depositing a **metal film** (2) on a starting substrate, which is selected from a single crystal sapphire substrate (1), a substrate comprising a single crystal **gallium nitride** film grown on a sapphire substrate and a single crystal semiconductor substrate;
(b) depositing a **gallium nitride** film (4) on the **metal film** to form a laminate substrate (5); and
(c) removing the starting substrate from the laminate substrate on which the **gallium nitride** film is deposited to form a free standing **gallium nitride** crystal substrate.
INDEPENDENT CLAIMS are also included for the following:
(i) a process for producing a **gallium nitride** crystal substrate comprising: depositing a **metal film** (2) on a starting substrate, which is selected from a single crystal sapphire substrate (1), a substrate comprising a single crystal **gallium nitride** film grown on a sapphire substrate and a

single crystal semiconductor substrate; forming a mask region and a **gallium nitride** selective growth region formed of a patterned mask material on the **metal film**; depositing, using the selective growth region as an origin, a **gallium nitride** film (4) on the selective growth region and the mask region to form a laminate substrate (5); and removing the starting substrate from the laminate substrate on which the **gallium nitride** film is deposited to form a free standing **gallium nitride** crystal substrate;

(ii) a process for producing a **gallium nitride** crystal substrate comprising: depositing a **metal film** (2) on a starting substrate, which is selected from a single crystal sapphire substrate (1), a substrate comprising a single crystal **gallium nitride** film grown on a sapphire substrate and a single crystal semiconductor substrate; depositing a **gallium nitride** film on the **metal film**; forming a mask region and a **gallium nitride** selective growth region formed of a patterned mask material on the **gallium nitride** film; depositing, using the selective growth region as an origin, a **gallium nitride** film (4) on the selective growth region and the mask region to form a laminate substrate (5); and removing the starting substrate from the laminate substrate on which the **gallium nitride** film is deposited to form a free standing **gallium nitride** crystal substrate;

(iii) a process for producing a **gallium nitride** crystal substrate comprising: forming a mask region and a **gallium nitride** selective growth region formed of a patterned mask material on a starting substrate which is selected from a single crystal sapphire substrate (1), a substrate comprising a single crystal **gallium nitride** film grown on a sapphire substrate and a single crystal semiconductor substrate; depositing, using the selective growth region as an origin, a **gallium nitride** film on the selective growth region and the mask region; forming a **metal film** (2) on the **gallium nitride** film; depositing a **gallium nitride** film (4) on the **metal film** to form a laminate substrate (5); and removing the starting substrate from the laminate substrate on which the **gallium nitride** film is deposited to form a free standing **gallium nitride** crystal substrate; and

(iv) a free standing **gallium nitride** crystal substrate obtained by one of the above processes.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view showing one preferred embodiment of an **epitaxially grown gallium nitride** laminate substrate to which the production process of a **gallium nitride** crystal substrate has been applied.

Single crystal sapphire c-face substrate 1

Metal film 2

Aluminum nitride film 3

Gallium nitride film 4

Laminate substrate 5

Dwg.1/5

L68 ANSWER 4 OF 46 WPIX (C) 2003 THOMSON DERWENT

AN 2002-652100 [70] WPIX

DNN N2002-516692 DNC C2002-183468

TI Self supported **gallium nitride** single crystal substrate used for light emitting devices has a specified diameter and contains no arsenic.

DC L03 U11 U12

PA (HITD) HITACHI CABLE LTD

CYC 1
PI JP 2002241198 A 20020828 (200270)* 6p
ADT JP 2002241198 A JP 2001-35449 20010213
PRAI JP 2001-35449 20010213
AB JP2002241198 A UPAB: 20021031
NOVELTY - A self supported **gallium nitride** single crystal substrate has a diameter of 50 mm or larger and contains no arsenic.
USE - The method produces the self supported **gallium nitride** single crystal substrate used for light emitting devices, including a light emitting diode, a semiconductor laser, electronic devices, including a high output field effect transistor.
ADVANTAGE - The self supported **gallium nitride** single crystal substrate exhibits simple handling and substantially forms no defects caused by the arsenic. A separation process for the **gallium nitride** layer and the substrate is simplified compared with the use of a sapphire substrate.
Dwg.0/2

L68 ANSWER 5 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 2002-434695 [46] WPIX
CR 2001-540886 [60]; 2002-239104 [29]; 2002-328205 [36]; 2002-328206 [36]; 2002-328347 [36]; 2002-403396 [43]; 2002-478915 [51]; 2002-506816 [54]; 2002-566148 [60]
DNN N2002-342194 DNC C2002-123361
TI Semiconductor structure for use in integrated circuits, includes monocrystalline compound semiconductor material formed on monocrystalline oxide material.
DC L03 U11
IN DROOPAD, R; HILT, L L; RAMDANI, J
PA (MOTI) MOTOROLA INC
CYC 3
PI US 2002047123 A1 20020425 (200246)* 26p
KR 2002075403 A 20021004 (200313)
TW 483050 A 20020411 (200313)
KR 2002077678 A 20021012 (200314)
KR 2002077907 A 20021014 (200314)
ADT US 2002047123 A1 Div ex US 2000-502023 20000210, US 2001-986034 20011107; KR 2002075403 A KR 2002-710317 20020809; TW 483050 A TW 2001-102847 20010209; KR 2002077678 A KR 2002-710309 20020809; KR 2002077907 A KR 2002-710310 20020809
PRAI US 2000-502023 20000210; US 2001-986034 20011107
AB US2002047123 A UPAB: 20030227
NOVELTY - A semiconductor structure comprises a monocrystalline oxide material and a monocrystalline compound semiconductor material of first type formed on the monocrystalline oxide material.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(a) A process for fabricating a semiconductor structure comprising providing a monocrystalline semiconductor substrate of silicon, **epitaxially growing** a monocrystalline oxide layer on the monocrystalline substrate, oxidizing the monocrystalline semiconductor substrate during **epitaxially growing** to form a silicon oxide layer between the substrate and the monocrystalline oxide layer and **epitaxially growing** a monocrystalline compound semiconductor layer on the monocrystalline oxide layer;
(b) A semiconductor device comprising a first monocrystalline semiconductor layer having regions, an electrical semiconductor component, a second monocrystalline compound semiconductor layer and second semiconductor component partially within the second semiconductor layer;and

(c) A communicating device comprising an integrated circuit which comprises an accommodating **buffer layer** (164), a compound semiconductor portion on the accommodating **buffer layer** and having feature of amplifier, modulating circuit or demodulating circuit, and a group IV semiconductor portion having a digital logic portion coupled to the feature.

USE - For use in integrated circuits useful for electronic devices.

ADVANTAGE - The structure provides a high quality monocrystalline compound semiconductor film on another monocrystalline material. It allows semiconductor device to be shrunk. It is fabricated with decrease manufacturing costs and with increased yield and reliability.

DESCRIPTION OF DRAWING(S) - The figure illustrates a cross-sectional views of a portion of an integrated circuit that includes a semiconductor laser and a metal oxide semiconductor transistor.

Intermediate layer 162

Buffer layer 164

Insulator layer 190

Dwg.18/18

L68 ANSWER 6 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 2002-426363 [45] WPIX
DNN N2002-335252 DNC C2002-120886
TI Electronic device such as microelectronic device or optoelectronic device, has alloy layer containing magnesium oxide and zinc oxide and/or cadmium oxide, and having cubic structure.
DC L02 L03 U11 U12
IN MUTH, J F; NARAYAN, J; SHARMA, A K
PA (MUTH-I) MUTH J F; (NARA-I) NARAYAN J; (SHAR-I) SHARMA A K; (UYNC-N) UNIV NORTH CAROLINA STATE
CYC 97
PI WO 2002031890 A2 20020418 (200245)* EN 35p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW
W: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
US 2002084466 A1 20020704 (200247)
AU 2001097025 A 20020422 (200254)
US 6423983 B1 20020723 (200254)
US 6518077 B2 20030211 (200314)
ADT WO 2002031890 A2 WO 2001-US42640 20011012; US 2002084466 A1 Div ex US 2000-687519 20001013, US 2002-50077 20020115; AU 2001097025 A AU 2001-97025 20011012; US 6423983 B1 US 2000-687519 20001013; US 6518077 B2 Div ex US 2000-687519 20001013, US 2002-50077 20020115
FDT AU 2001097025 A Based on WO 200231890; US 6518077 B2 Div ex US 6423983
PRAI US 2000-687519 20001013; US 2002-50077 20020115
AB WO 200231890 A UPAB: 20020717

NOVELTY - An electronic device has an alloy layer (18) comprising (a) magnesium oxide and (b) zinc oxide and/or cadmium oxide, on a substrate (12). The alloy has cubic structure.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Fabrication of microelectronic device which involves forming an alloy layer comprising magnesium oxide (MgO) and zinc oxide and/or cadmium oxide, on a support; and

(2) An alloy comprising magnesium and zinc oxide and/or cadmium oxide, and having cubic structure.

USE - As optoelectronic device such as light emitting diode, laser diode, photodetectors and windows that are transparent to ultraviolet radiation, optical modulators and broad band light sources such as light

bulbs; or microelectronic device such as transistors, field emitters and power devices, which are used in consumer and commercial application.

ADVANTAGE - Electronic devices have wider band gap, increased binding energy of excitons and/or reduced density of growth and/or misfit dislocation compared with conventional III-nitride-electronic devices. The design of electronic material permit tailoring of band gaps which may allow control of optoelectronic properties in the visible and ultraviolet range and provides for integration with silicon microelectronic devices.

DESCRIPTION OF DRAWING(S) - The figure shows cross-sectional view of electronic device.

Substrate 12

Alloy layer 18

Dwg.1/11

L68 ANSWER 7 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 2002-388352 [42] WPIX
DNN N2002-304334 DNC C2002-109838
TI Semiconductor element for ultraviolet semiconductor laser, has **aluminum nitride** layer, **gallium nitride** layer and **boron nitride** layer which are laminated alternately.
DC L03 U11 U12 V08
PA (NITE) NIPPON TELEGRAPH & TELEPHONE CORP
CYC 1
PI JP 2002075873 A 20020315 (200242)* 5p
ADT JP 2002075873 A JP 2000-255251 20000825
PRAI JP 2000-255251 20000825
AB JP2002075873 A UPAB: 20020704

NOVELTY - The **aluminum nitride buffer layer** (2), a GaN **epitaxial growth** layer (3) and **boron nitride** (BN) layer are laminated alternately on the sapphire substrate or 6H-SiC substrate.

USE - Semiconductor element for ultraviolet semiconductor laser, high frequency power device, high temperature operation device, etc.

ADVANTAGE - Improves visualization property by enabling rearrangement of GaN **epitaxial growth** layer.

DESCRIPTION OF DRAWING(S) - The figure shows the explanation of the effect of the semiconductor elements. (Drawing includes non-English language text).

Aluminum nitride buffer layer

2

GaN **epitaxial growth** layer 3

Dwg.2/3

L68 ANSWER 8 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 2002-268986 [31] WPIX
DNN N2002-209361 DNC C2002-079780
TI Giant magneto-resistive spin valve structure for, e.g., non-volatile memory elements comprises multiple layers of ferromagnetic material monolithically integrated with silicon circuits.
DC L03 T03 U12 U14 V02
IN EISENBEISER, K; FINDER, J M
PA (MOTI) MOTOROLA INC
CYC 94
PI WO 2002009126 A2 20020131 (200231)* EN 46p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW
W: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW

AU 2001075978 A 20020205 (200236)
ADT WO 2002009126 A2 WO 2001-US22649 20010718; AU 2001075978 A AU 2001-75978 20010718
FDT AU 2001075978 A Based on WO 200209126
PRAI US 2000-624690 20000724
AB WO 200209126 A UPAB: 20020516
NOVELTY - Giant magnetoresistive (GMR) spin valve structure (20) having multiple layers of a ferromagnetic material (26, 30) and a conductive nonmagnetic material (28) can be monolithically integrated with silicon circuits by growing an accommodating **buffer layer** (24) on a silicon wafer (22) via a strain-reducing amorphous silicon oxide layer (32).

DETAILED DESCRIPTION - The spin valve structure (20) comprises, in sequence, a monocrystalline semiconductor substrate, a monocrystalline insulator layer, an **epitaxially-grown** first layer (26) capable of exhibiting ferromagnetic properties, an **epitaxially-grown** second electrically conductive, nonmagnetic layer (28), and a third layer (30) capable of exhibiting ferromagnetic properties.

Preferred Features: The first, second and third layers are preferably monocrystalline. An amorphous oxide layer underlies the first layer. A CMOS circuit can formed at least partially in the substrate. An integrated logic element can be formed in the substrate, the first, second and third layers can be patterned to form a magnetic sensor, preferably a memory element, which can be interconnected to the integrated logic element.

INDEPENDENT CLAIMS are given for:

(a) an integrated spin valve circuit having an amorphous oxide layer between a first monocrystalline oxide layer and an integrated logic circuit formed on a silicon substrate;

(b) processes for fabricating spin valve and integrated spin valve circuits; and

(c) a process for fabricating a spin valve.

USE - Production of magneto-electronic devices, such as non-volatile memory elements and read/write heads for disk drives.

ADVANTAGE - GMR materials can be monolithically integrated into standard CMOS (or similar integrated circuit) processes, to provide high GMR spin valves.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section of a portion of a spin valve structure.

Spin valve structure 20
Monocrystalline structure 22
Accommodating **buffer layer** 24
Ferromagnetic layers 26, 30
Conductive nonmagnetic layer 28
Template layer 34
Magnetic vectors 34, 36

Dwg.1/12

L68 ANSWER 9 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 2002-239745 [29] WPIX
DNN N2002-184916 DNC C2002-072259
TI Group three nitride compound semiconductor is formed by etching a sapphire substrate to form a stripe pattern, forming an **aluminum nitride buffer layer** and forming a **gallium nitride** layer by vertical and horizontal **epitaxial growth**.
DC L03 U11 U12 V08
IN TEZEN, Y
PA (TOZA) TOYODA GOSEI KK
CYC 95
PI WO 2001069662 A1 20010920 (200229)* JA 49p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ

NL OA PT SD SE SL SZ TR TZ UG ZW
W: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM
DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS KE KG KP KR KZ LC LK
LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG
SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
AU 2001034169 A 20010924 (200229)
JP 2001267242 A 20010928 (200229) 18p
EP 1265272 A1 20021211 (200301) EN
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT
RO SE SI TR
ADT WO 2001069662 A1 WO 2001-JP1396 20010223; AU 2001034169 A AU 2001-34169 20010223; JP 2001267242 A JP 2000-71350 20000314; EP 1265272 A1 EP 2001-906290 20010223, WO 2001-JP1396 20010223
FDT AU 2001034169 A Based on WO 200169662; EP 1265272 A1 Based on WO 200169662
PRAI JP 2000-71350 20000314
AB WO 200169662 A UPAB: 20020508
NOVELTY - Group three nitride compound semiconductor is formed by etching a sapphire substrate to form a stripe pattern, forming an **aluminum nitride buffer layer** on the top and bottom surfaces of a step on the substrate and forming a **gallium nitride** layer by vertical and horizontal **epitaxial growth**.

DETAILED DESCRIPTION - A sapphire substrate (1) is etched in a stripe pattern having a width of 10 microns, an interval of 10 microns, and a depth of 10 microns. An **aluminum nitride buffer layer** (2) with a thickness of about 40 nm is formed mainly on the top and bottom surfaces of a step on the substrate (1). A **gallium nitride** layer (3) is formed by vertical and horizontal **epitaxial growth**. Thus the step is covered by the **buffer layer** (21) grown on the top surface of the step by horizontal epitaxy, and therefore the surface is planarized. The threading dislocations in the portion of the **gallium nitride** layer (3) above the bottom of the step are significantly suppressed compared with the portion of it above the top of the step.

USE - None given.

DESCRIPTION OF DRAWING(S) - The drawing illustrates the method.
Substrate 1
Buffer layers 2, 21
Gallium nitride layer 3
1a, 1b, 1c, 1d/18

L68 ANSWER 10 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 2002-235445 [29] WPIX
DNN N2002-180772 DNC C2002-071450
TI **Gallium nitride** epilayer production on sapphire substrate, uses molecular beam epitaxy with magnetron sputter **epitaxy grown aluminum nitride buffer layer**.
DC L03 U11
IN TANG, H; WEBB, J
PA (CANA) NAT RES COUNCIL CANADA
CYC 1
PI US 6291318 B1 20010918 (200229)* 5p
ADT US 6291318 B1 US 1999-412395 19991005
PRAI US 1999-412395 19991005
AB US 6291318 B UPAB: 20020508
NOVELTY - A **gallium nitride** epilayer is formed on a sapphire substrate by growing an **aluminum nitride buffer layer** on the substrate by magnetron sputter epitaxy to reduce lattice mismatch, and forming the **gallium**

nitride epilayer on the **buffer layer**.
USE - The method is used for the production of a **gallium nitride** epilayer on sapphire. The **gallium nitride** can be used in a light emitting diode, e.g. blue laser diodes. It can also be used in high power microwave metal-semiconductor field-effect transistors and modulation doped field-effect transistors.
ADVANTAGE - The method reduces the defects affecting the electron mobility and the **gallium nitride** layer can be grown with good reproducibility.
Dwg.0/3

L68 ANSWER 11 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 2002-229661 [29] WPIX
DNN N2002-176635 DNC C2002-069843
TI Photonic device, such as light-emitting device and photodetector, includes **buffer layer** of specified composition and multi-layered thin film of specified composition.
DC L03 U12
IN ASAI, K; NAGAI, T; SHIBATA, T; TANAKA, M
PA (NIGA) NGK INSULATORS LTD
CYC 30
PI EP 1160882 A2 20011205 (200229)* EN 13p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
US 2002020850 A1 20020221 (200229)
KR 2001107604 A 20011207 (200236)
CN 1344037 A 20020410 (200249)
JP 2002176196 A 20020621 (200256) 10p
JP 2002176197 A 20020621 (200256) 9p
US 6495894 B2 20021217 (200307)
ADT EP 1160882 A2 EP 2001-112409 20010521; US 2002020850 A1 US 2001-854925 20010514; KR 2001107604 A KR 2001-27650 20010521; CN 1344037 A CN 2001-137289 20010522; JP 2002176196 A JP 2001-114065 20010412; JP 2002176197 A JP 2001-114067 20010412; US 6495894 B2 US 2001-854925 20010514
PRAI JP 2001-114067 20010412; JP 2000-149190 20000522; JP 2000-149191 20000522; JP 2000-293763 20000927; JP 2000-293846 20000927; JP 2001-114065 20010412
AB EP 1160882 A UPAB: 20020508
NOVELTY - A photonic device e.g. light-emitting device includes a substrate, a **buffer layer** containing **aluminum -gallium-indium nitride**, and a multi-layered thin film comprising **aluminum-gallium-indium nitride**.
The **aluminum** content of **aluminum** component-minimum portion of the **buffer layer** is greater than at least the thickest layer of the multi-layered thin film.
DETAILED DESCRIPTION - A photonic device e.g. light-emitting device consists of a substrate (1), a **buffer layer** (2) formed on the substrate, and a multi-layered thin film (6-8) **epitaxially grown** on the **buffer layer**. The **buffer layer** comprises **aluminum-gallium-indium nitride** (A1GabIncN), and the multi-layered thin film contains **aluminum-gallium-indium nitride** (AlxGayInzN) (where (a + b + c) = 1; (x + y + z) = 1; and a, b, c, x, y, z = greater than 0). The **aluminum** (**Al**) content of **Al** component-minimum portion of the **buffer layer** is larger than at least the thickest layer of the multi-layered thin film. The **Al** component of the **buffer layer** decreases continuously or stepwise from the side of the substrate to the side of the multi-layered thin film.

An INDEPENDENT CLAIM is also included for a method of fabricating a photonic device by preparing a substrate, forming a **buffer layer** by metal-organic chemical vapor deposition (MOCVD), and **epitaxially growing** a multi-layered thin film by MOCVD.

USE - As e.g. light-emitting device and photodetector.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of the photonic device.

Substrate 1

Buffer layers 2

Multi-layered thin film 6-8

Dwg.6/7

L68 ANSWER 12 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 2001-628255 [73] WPIX
DNN N2001-468538 DNC C2001-187227
TI High power optoelectronic device made by forming metal grid on semiconductor substrate, applying non nucleating, non spread layer to grid and then growing semiconductor layer.
DC L03 U11 U12
IN GARCIA, J C; GUYAUX, J L; MASSIES, J
PA (CSFC) THOMSON CSF SA
CYC 1
PI FR 2803433 A1 20010706 (200173)* 14p
ADT FR 2803433 A1 FR 1999-16766 19991230
PRAI FR 1999-16766 19991230
AB FR 2803433 A UPAB: 20011211
NOVELTY - Manufacture of a semiconductor device includes forming a metal grid in a semiconductor substrate by using a mask to form openings, depositing a **metal layer** and removing the mask and metal formed on it. A layer that does not nucleate or spread is applied to the grid and then a semiconductor material is grown epitaxially across the substrate.

DETAILED DESCRIPTION - Both semiconductor materials may be **gallium nitride**. The layer on top of the grid may be formed by oxidizing, or nitriding the metal or by encapsulating the metal in dielectric. The **epitaxial growth** takes place at least 800 deg. C.

USE - Semiconductors, particularly high power opto-electronic devices.

ADVANTAGE - Use of a **gallium nitride** substrate is made possible.

DESCRIPTION OF DRAWING(S) - The drawing shows a semiconductor device. (The drawing includes non-English language text).

Dwg.6/6

L68 ANSWER 13 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 2001-282115 [29] WPIX
DNN N2001-201053 DNC C2001-086047
TI Fabrication of a **gallium nitride**-based semiconductor structure on a substrate, e.g. in manufacture of blue light-emitting diodes, laser diodes and high speed high power transistor devices, involves single step pendeo and lateral overgrowth.
DC L03 U11 U12
IN EDMOND, J A; EMERSON, D T; HABERERN, K W; KONG, H
PA (CREE-N) CREE INC; (EDMO-I) EDMOND J A; (EMER-I) EMERSON D T; (HABE-I) HABERERN K W; (KONG-I) KONG H
CYC 92
PI WO 2001027980 A1 20010419 (200129)* EN 47p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TZ UG ZW
W: AE AG AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CZ DE DK DM DZ EE

ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KR KZ LC LK LR LS
LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK
SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
AU 2000080095 A 20010423 (200147)
US 2002022290 A1 20020221 (200221)
EP 1222685 A1 20020717 (200254) EN
R: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO
SE SI
US 2002098693 A1 20020725 (200254)
KR 2002047225 A 20020621 (200280)
CN 1378702 A 20021106 (200316)

ADT WO 2001027980 A1 WO 2000-US28056 20001011; AU 2000080095 A AU 2000-80095 20001011; US 2002022290 A1 Provisional US 1999-159299P 19991014, Cont of US 2000-679799 20001005, US 2001-934270 20010821; EP 1222685 A1 EP 2000-970767 20001011, WO 2000-US28056 20001011; US 2002098693 A1 Provisional US 1999-159299P 19991014, Div ex US 2000-679799 20001005, US 2002-56607 20020124; KR 2002047225 A KR 2002-704609 20020410; CN 1378702 A CN 2000-814189 20001011

FDT AU 2000080095 A Based on WO 200127980; EP 1222685 A1 Based on WO 200127980

PRAI US 1999-159299P 19991014; US 2000-679799 20001005; US 2001-934270 20010821; US 2002-56607 20020124

AB WO 200127980 A UPAB: 20010528

NOVELTY - Mask having an opening is formed on a substrate, and an epitaxial layer **gallium nitride** or Group III nitride alloys of **gallium nitride** is grown vertically from the opening and laterally across the mask. The lateral growth rate of the layer is maintained at a rate sufficient to prevent polycrystalline nitride material nucleating on the mask from interrupting the lateral growth of the layer.

DETAILED DESCRIPTION - The ratio of the lateral growth rate to the vertical growth rate is preferably greater than 1:1, and the lateral growth rate is 2-8 microns/hour.

The substrate preferably comprises silicon carbide.

A **buffer layer** comprising AlxGa1-xN (x = 0-1), which forms a conductive interface to the substrate, can be grown through the opening in the mask to support the **epitaxial growth** of Group III nitrides.

INDEPENDENT CLAIMS are given for:

(a) methods of fabrication of a **gallium nitride**-based semiconductor structure on a substrate;

(b) a semiconductor structure; and

(c) a **gallium nitride**-based semiconductor structures.

USE - Fabrication of Group III-nitride semiconductor structures by pendeo and lateral epitaxial overgrowth, e.g. for manufacture of blue light-emitting diodes, laser diodes and high speed high power transistor devices.

ADVANTAGE - A relatively defect-free single crystal film of **gallium nitride** can be fabricated in a single step process without having to minimize nucleation on a mask.

DESCRIPTION OF DRAWING(S) - The drawings show cross-sections of a substrate on which (a) a pair of raised portions have been formed and a mask layer has been deposited, and (b) a pair of raised portions have been formed and a mask layer has been deposited using a self alignment technique.

Substrate 10
Buffer layer 12
Mask 14
Raised portion 15
Openings 16
Trenches 18

Etch mask 19
6A, 6B/16

L68 ANSWER 14 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 2001-128210 [14] WPIX
DNN N2001-094678 DNC C2001-038162
TI Semiconductor device manufacturing method e.g for light emitting diode, involves depositing thin **metal film** over N-type **gallium nitride** layer after dissolving P-type **gallium nitride** layer in atomic hydrogen.
DC L03 U12
PA (SANK-N) SANKEN DENKI KK
CYC 1
PI JP 2000315818 A 20001114 (200114)* 12p
ADT JP 2000315818 A JP 1999-124610 19990430
PRAI JP 1999-124610 19990430
AB JP2000315818 A UPAB: 20010312
NOVELTY - P-type GaN group compound layer is **epitaxially grown** on substrate (11) at predetermined temperature in hydrogen atmosphere. N-type GaN group compound layer is grown above P-type layer at temperature higher than previous temperature. The P-type layer is dissolved in atomic hydrogen at predetermined temperature and thin **metal film** is deposited over N-type layer.
USE - For manufacturing semiconductor light emitting element such as light emitting diode, semiconductor laser or transistor.
ADVANTAGE - P-type layer with low resistance factor is formed by dissolving P-type **gallium nitride** group compound layer in atomic hydrogen.
DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of manufacturing method of semiconductor light emitting elements.
Substrate 11
Dwg.1/5

L68 ANSWER 15 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 2000-674282 [66] WPIX
DNN N2000-499896 DNC C2000-204509
TI Manufacture of Group III nitride compound semiconductor for light emitting device involves forming island pattern **buffer layer** on substrate.
DC L03 U11 U12 V08
IN KOIKE, M; NAGAI, S
PA (TOZA) TOYODA GOSEI KK; (KOIK-I) KOIKE M; (NAGA-I) NAGAI S
CYC 27
PI EP 1052684 A1 20001115 (200066)* EN 16p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 2000323417 A 20001124 (200109) 8p
US 2002179005 A1 20021205 (200301)
ADT EP 1052684 A1 EP 2000-109798 20000509; JP 2000323417 A JP 1999-129322 19990510; US 2002179005 A1 Div ex US 2000-566917 20000509, US 2002-187943 20020702
PRAI JP 1999-129322 19990510
AB EP 1052684 A UPAB: 20001219
NOVELTY - The method comprises forming a **buffer layer** (2) in the form of an island pattern on a substrate (1), and growing a Group III nitride compound semiconductor layer (3) epitaxially in longitudinal and lateral directions.
DETAILED DESCRIPTION - The method comprises
(i) forming a **buffer layer** (2) in the form of an island pattern on a substrate (1), the pattern being dot, striped or grid pattern such that substrate exposed portions are formed in a scattered

manner, and
(ii) growing a Group III nitride compound semiconductor layer (3) on the patterned **buffer layer** epitaxially in longitudinal and lateral directions.
Preferred method: The semiconductor layer is etched and further compound semiconductor is **epitaxially grown** on the unetched portion of the semiconductor layer. The **buffer layer** is made of **aluminium nitride**. the substrate is made of sapphire.
An INDEPENDENT CLAIM is included for a light emitting Group III nitride semiconductor device.
USE - For light emitting device such as laser and light emitting diodes.
ADVANTAGE - Provides a Group III nitride semiconductor layer having little or no feedthrough dislocations. The semiconductor layer has excellent crystallinity resulting in improved device characteristics.
DESCRIPTION OF DRAWING(S) - The drawings show processing steps during the manufacture of the semiconductor layer.
Substrate 1
Buffer layer 2
Semiconductor 3
Dislocations 4
Gallium nitride regions 31,32
Dwg.1A-D/6

L68 ANSWER 16 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 2000-527925 [48] WPIX
DNN N2000-390407 DNC C2000-157127
TI Nitride group compound semiconductor element, such as light emitting diode, has a substrate provided with a **boron nitride** group semiconductor **buffer layer** and a nitride group compound semiconductor crystal layer.
DC L03 U11 U12
IN OH, M S; WON, J H
PA (SANS-N) SANSEI DENKI KK; (SMSU) SAMSUNG ELECTRICS CO LTD; (SMSU) SAMSUNG ELECTRO MECHANICS CO LTD
CYC 3
PI JP 2000188260 A 20000704 (200048)* 16p
KR 2000041281 A 20000715 (200113)
TW 429553 A 20010411 (200157)
ADT JP 2000188260 A JP 1999-332030 19991122; KR 2000041281 A KR 1998-57119 19981222; TW 429553 A TW 1999-119726 19991111
PRAI KR 1998-57119 19981222
AB JP2000188260 A UPAB: 20001001
NOVELTY - A **buffer layer** (24) comprising **boron nitride** (BN) compound semiconductor is formed on a substrate (11). A nitride group compound semiconductor crystal layer (34) is arranged on the **buffer layer**, to form a nitride group compound semiconductor element.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(i) Crystal growth of nitride group compound semiconductor involves forming BN group compound semiconductor **buffer layer** on the substrate at predetermined temperature followed by **epitaxial growth** of nitride group semiconductor crystal layer on the **buffer layer** at a temperature higher than the temperature for **buffer layer** formation;
(ii) Manufacture of nitride group compound semiconductor element involves **epitaxial growth** of BN group semiconductor layer to form **buffer layer** on the substrate, forming n-type nitride group compound semiconductor crystal layer (34) on

buffer layer, growing the nitride group semiconductor crystal to form an activated layer (35) and finally forming a p-type nitride group compound semiconductor crystal layer (36) on the activated layer. Thus, a laminate of p-n joint structure of nitride group compound semiconductor crystal layer is formed on **buffer layer**.
A pair of electrodes (41,42) are provided for impressing voltage to the activated layer.

USE - None given.

ADVANTAGE - The **buffer layer** relieves the lattice mismatching between substrate and nitride group semiconductor crystal layers. Therefore, the crystallinity of nitride group compound semiconductor single crystal layer is improved. Light-emission property, electrical property and durability of the semiconductor light-emitting element such as light-emitting diode, are improved.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional drawing of the structure of a blue light-emitting diode.
Substrate 11
BN group compound **buffer layer** 24
n-type nitride group compound semiconductor crystal layer 34
Activated layer 35
p-type nitride group compound semiconductor crystal layer 36
Electrodes 41, 42
Dwg.2/9

L68 ANSWER 17 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 2000-441898 [38] WPIX
DNN N2000-329826 DNC C2000-134160
TI Fabrication of a **gallium nitride** microelectronic layer for microelectronic devices, e.g. transistor, by **epitaxially growing** silicon carbide layer on a silicon surface, and laterally growing the **gallium nitride** layer.
DC L03 U11 U12
IN DAVIS, R F; GEHRKE, T; LINTHICUM, K J; THOMSON, D B; TRACY, K M
PA (UYNC-N) UNIV NORTH CAROLINA STATE; (DAVI-I) DAVIS R F; (GEHR-I) GEHRKE T; (LINT-I) LINTHICUM K J; (THOM-I) THOMSON D B; (TRAC-I) TRACY K M
CYC 86
PI WO 2000031783 A1 20000602 (200038)* EN 62p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW
W: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZA ZW
AU 2000021520 A 20000613 (200043)
US 6255198 B1 20010703 (200140)
US 2002031851 A1 20020314 (200222)
ADT WO 2000031783 A1 WO 1999-US27358 19991118; AU 2000021520 A AU 2000-21520 19991118; US 6255198 B1 Provisional US 1998-109674P 19981124, Provisional US 1998-109860P 19981124, US 1999-441754 19991117; US 2002031851 A1 Provisional US 1998-109674P 19981124, Provisional US 1998-109860P 19981124, Cont of US 1999-441754 19991117, US 2001-850687 20010507
FDT AU 2000021520 A Based on WO 200031783; US 2002031851 A1 Cont of US 6255198
PRAI US 1998-109860P 19981124; US 1998-109674P 19981124; US 1999-441754 19991117; US 2001-850687 20010507
AB WO 200031783 A UPAB: 20000811
NOVELTY - **Gallium nitride** microelectronic layer is fabricated by converting a surface of a silicon substrate to 3C-silicon carbide, which is **epitaxially grown** on the silicon layer surface. A layer of 2H-**gallium nitride** is then grown on the 3C-silicon carbide layer and laterally grown to produce the **gallium nitride** microelectronic layer.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a **gallium nitride** microelectronic structure comprising a silicon layer with the 3C-silicon carbide layer, an underlying 2H-**gallium nitride** layer on the silicon carbide layer, and a lateral layer of the underlying 2H-**gallium nitride**.

USE - For fabricating a **gallium nitride** microelectronic layer for microelectronic devices, e.g. transistor, field emitters and optoelectronic devices.

ADVANTAGE - The method provides low cost and/or high availability **gallium nitride** devices that can be integrated with conventional complimentary metal oxide semiconductors (CMOS) and other silicon technologies.

Dwg.0/49

L68 ANSWER 18 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 2000-127503 [12] WPIX
CR 2000-098657 [09]; 2000-107214 [09]; 2000-107215 [09]; 2000-127762 [09]
DNN N2000-096061 DNC C2000-039083
TI Single crystal **aluminum nitride** layers, useful as high frequency SAW filters and **buffer layers** for electronic and optoelectronics component deposition, are grown on silicon using silicon surface construction and reconstruction steps.
DC L03 U11 U13
IN KIPSHIDZE, G D; RICHTER, W; SCHENK, H P
PA (RICH-I) RICHTER W
CYC 1
PI DE 19827198 A1 20000120 (200012)* 4p
ADT DE 19827198 A1 DE 1998-19827198 19980618
PRAI DE 1998-19827198 19980618
AB DE 19827198 A UPAB: 20000308

NOVELTY - Single crystal **aluminum nitride** layer molecular beam **epitaxial growth** on silicon comprises silicon surface construction and reconstruction steps.

DETAILED DESCRIPTION - Single crystal **aluminum nitride** layers are produced on silicon by:

(a) placing a single crystal silicon wafer (2) with a clean Si(111) surface (3), an **Al** molecular beam source (4), an activated nitrogen source (5) and a RHEED electron diffraction unit (6) in an MBE growth chamber (1);

(b) forming a Si(111)-(7x7) surface construction on the wafer surface at elevated temperature under ultrahigh vacuum conditions;

(c) heating the wafer to the nucleation temperature of 600-800 deg. C;

(d) either directing an atomic nitrogen flow onto the wafer surface for rapid achievement of a 3x3 surface reconstruction and then initiating a similar size flow of **Al** or directing an **Al** flow onto the wafer surface for rapid achievement of a 43x43 surface reconstruction and then initiating a similar size flow of atomic nitrogen; and

(e) gradually heating the wafer to 850-950 deg. C while directing a constant flow of atomic nitrogen onto the wafer and adjusting the **Al** flow so that a 32x32, 1x1 or 2x6 reconstruction is observed in the electron diffraction image.

USE - For producing single crystal **aluminum nitride** layers useful as h.f. surface acoustic wave (SAW) filters and as **buffer layers** for subsequent deposition of electronic and optoelectronics components based on AlxGa1-xN and InxGa1-xN.

ADVANTAGE - The process permits growth of single crystal AlN layers with high perfection and smooth surfaces on inexpensive silicon substrates in spite of the large lattice mismatch between Si(111) and AlN(0001).

DESCRIPTION OF DRAWING(S) - The drawing shows a schematic view of suitable coating equipment for carrying out the process of the invention.

MBE growth chamber 1
Silicon wafer 2
Wafer surface 3
Molecular beam source 4
Activated nitrogen source 5
Electron diffraction unit 6
Dwg.1/1

L68 ANSWER 19 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 1999-625570 [54] WPIX
DNN N1999-462311 DNC C1999-182728
TI Multilayer epitaxial film formation for optical discharge device - involves forming **metal layer** and **epitaxially grown** single crystal semiconductor layer sequentially over insulating substrate.
DC L03 U11 U13
IN FUKE, S; SUMIYA, M; YOSHIMOTO, M
PA (UYSH-N) UNIV SHIZUOKA
CYC 2
PI JP 11274561 A 19991008 (199954)* 7p
US 6239005 B1 20010529 (200132)
ADT JP 11274561 A JP 1998-77140 19980325; US 6239005 B1 US 1999-275453 19990324
PRAI JP 1998-77140 19980325
AB JP 11274561 A UPAB: 20000105
NOVELTY - Above sapphire-made single crystal insulating substrate (10), a platinum layer (11) is deposited on [111] plane of C surface. A **gallium nitride** semiconductor layer (12) with single crystal structure is grown on the metal surface by epitaxial method.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for optical discharge semiconductor device manufacture method.
USE - For optical discharge device like blue semiconductor laser.
ADVANTAGE - Enables forming single crystal semiconductor layer directly on **metal layer**.
DESCRIPTION OF DRAWING - The diagram is a sectional view of semiconductor laser. (10) Substrate; (11) Platinum layer; (12) **Gallium nitride** semiconductor layer.
Dwg.2/6

L68 ANSWER 20 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 1999-333512 [28] WPIX
DNN N1999-251142 DNC C1999-098577
TI LED structure using III group nitride semiconductor - has reaction prevention electric conduction **buffer layer** which consists of silicon layer or **indium nitride** layer, interposed between germanium board and **aluminium-gallium -indium nitride** film of specified composition.
DC L03 U12 V08
PA (FJIE) FUJI ELECTRIC CO LTD
CYC 1
PI JP 11121800 A 19990430 (199928)* 6p
ADT JP 11121800 A JP 1997-293591 19971009
PRAI JP 1997-293591 19971009
AB JP 11121800 A UPAB: 19990719
NOVELTY - Reaction prevention electric conduction **buffer layer** (2c) which consists of Si layer or InN layer is interposed between Ge board (1g) and AlxGayIn1-x-yN film. The thickness of Si layer is between 1 nm and 1000 nm. DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for manufacturing method of light emitting diode using III group nitride semiconductor.
USE - For performing **epitaxial growth** on Ge board

of insulator.
ADVANTAGE - Differential thermal expansion between Ge board and AlxGayIn1-x-yN film is reduced by **buffer layer** and hence distortion of AlxGayIn1-x-yN film is minimized. Generation of void is prevented, thus ensuring uniform current flow. Improves manufacturing yield. DESCRIPTION OF DRAWING(S) - The figure shows sectional view of light emitting diode with Si reaction prevention electric conduction **buffer layer**. (1g) Ge board; (2c) **Buffer layer**.
Dwg.1/6

L68 ANSWER 21 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 1999-294278 [25] WPIX
DNN N1999-220855 DNC C1999-086817
TI Nitride group semiconductor light emitting device for digital information recording device e.g. magneto-optical disc - includes light shading layers in which compositions of **aluminium gallium nitride** are identical.
DC L03 T03 U12 V08 W04
PA (FUIT) FUJITSU LTD
CYC 1
PI JP 11097803 A 19990409 (199925)* 5p
ADT JP 11097803 A JP 1997-259651 19970925
PRAI JP 1997-259651 19970925
AB JP 11097803 A UPAB: 19990630
NOVELTY - The **epitaxial growth** layer extending from boundary surface of SiC substrate (11) to **buffer layer** (12) lies with an area ranging from 0.2-0.4 micrometers. The **buffer layer** composition is n-Al0.1Ga0.9N. Light shading layers (15,17) formed on **buffer layer** have identical compositions, i.e. p-Al0.05Ga0.95N.
USE - In digital information recording device, e.g. magneto- optical disc.
ADVANTAGE - Surface condition of **epitaxial growth** layer is maintained satisfactorily, thereby distortion exerted on barrier layer or light shading layer can be suppressed. The development of crystal defect is restricted.
DESCRIPTION OF DRAWING(S) - The figure shows principal part front elevation of semiconductor laser. (11) Substrate; (12) **Buffer layer**; (15,17) Light shading layers.
Dwg.1/2

L68 ANSWER 22 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 1999-257122 [22] WPIX
DNN N1999-191602 DNC C1999-075463
TI Growth of Group III-V nitride semiconductor **buffer layer** by molecular beam epitaxy.
DC L03 U11
IN HOOPER, S E
PA (SHAF) SHARP KK
CYC 22
PI GB 2331307 A 19990519 (199922)* 17p
WO 9925907 A1 19990527 (199928) EN
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: CA JP KR US
EP 1038056 A1 20000927 (200048) EN
R: DE FR GB
US 6270574 B1 20010807 (200147)
JP 2001523633 W 20011127 (200204) 21p
EP 1038056 B1 20020612 (200239) EN
R: DE FR GB

DE 69806054 E 20020718 (200255)
ADT GB 2331307 A GB 1997-24091 19971115; WO 9925907 A1 WO 1998-JP5129 19981113; EP 1038056 A1 EP 1998-953046 19981113, WO 1998-JP5129 19981113; US 6270574 B1 WO 1998-JP5129 19981113, US 2000-554534 20000714; JP 2001523633 W WO 1998-JP5129 19981113, JP 2000-521264 19981113; EP 1038056 B1 EP 1998-953046 19981113, WO 1998-JP5129 19981113; DE 69806054 E DE 1998-606054 19981113, EP 1998-953046 19981113, WO 1998-JP5129 19981113
FDT EP 1038056 A1 Based on WO 9925907; US 6270574 B1 Based on WO 9925907; JP 2001523633 W Based on WO 9925907; EP 1038056 B1 Based on WO 9925907; DE 69806054 E Based on EP 1038056, Based on WO 9925907
PRAI GB 1997-24091 19971115
AB GB 2331307 A UPAB: 19990609
NOVELTY - Growth of a **gallium nitride buffer layer** takes place at 600-700 deg. C, using ammonia as a nitrogen precursor species, on a sapphire substrate.

DETAILED DESCRIPTION - Group III-V nitride **buffer layer** is grown on a substrate (S) made of different material, by molecular beam epitaxy (MBE). The substrate is placed in a vacuum chamber (10) at reduced pressure and 300-800 deg. C. Species are supplied to the chamber, including a nitrogen precursor species supplying nitrogen to the substrate at a rate to cause **epitaxial growth** at a rate of 2-10 microns m/hour, forming a **buffer layer** less than 200 microns m thick.

Preferred Features: The substrate is sapphire. A species containing at least one Group III element, preferably **gallium**, **aluminum**, or **indium** is used, and the nitrogen precursor species is ammonia. An optoelectronic device is grown on the **buffer layer**.

USE - Growing a **buffer layer** to compensate for lattice mismatching between the substrate material and the epilayer material.

ADVANTAGE - **Buffer layer** growth rates of over 2 microns m/hour, and preferably 3-6 microns m/hour, are achieved by use of a higher temperature.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic diagram of apparatus for the MBE method.

vacuum chamber 10
heated support 12
vacuum pump 14
exhaust conduit 16
vacuum outlet 18
first supply conduit 20
outlet 22
effusion cells 24,26
substrate S
Dwg.1/4

L68 ANSWER 23 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 1998-146622 [14] WPIX
DNN N1998-116097 DNC C1998-047962
TI Continuous epitaxy of nitrogen-containing semiconductor layers - of different compositions by varying nitrogen supply.
DC L03 U11 U12 V08
IN AVERBECK, R; SCHIENLE, M; TEWS, H
PA (SIEI) SIEMENS AG
CYC 21
PI DE 19652548 C1 19980312 (199814)* 3p
EP 849380 A2 19980624 (199829) DE
R: AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
JP 10189453 A 19980721 (199839) 3p
US 5980631 A 19991109 (199954)

TW 423190 A 20010221 (200138)
ADT DE 19652548 C1 DE 1996-19652548 19961217; EP 849380 A2 EP 1997-118284 19971021; JP 10189453 A JP 1997-345087 19971215; US 5980631 A US 1997-992182 19971217; TW 423190 A TW 1997-119055 19971217
PRAI DE 1996-19652548 19961217
AB DE 19652548 C UPAB: 19980406
A process for **epitaxial growth** of semiconductor layers, having different solid solution compositions of nitrogen and one or more of **Al**, **Ga** and In, involves changing the quantity of nitrogen supplied per unit time during growth changeover from one layer to the next.

USE - Especially for producing abrupt interfaces between ternary nitrogen-containing III-V semiconductor layers by molecular beam epitaxy in the production of optoelectronic devices (such as lasers and LEDs), e.g. multiple quantum well structures (e.g. of In-**Ga-N**) in the active regions of lasers or superlattice structures (e.g. alternating **Al-Ga-N** and **Ga-N** thin films) as **buffer layers**.

ADVANTAGE - The process requires a minimal number of material sources and allows continuous successive growth of different layers using constant supplies of **Al**, **Ga** and In, only the nitrogen supply needing to be varied.

Dwg.0/0

L68 ANSWER 24 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 1997-492006 [46] WPIX
DNN N1997-409507 DNC C1997-157035
TI Vapour phase epitaxy of **indium-gallium-nitride** compound semiconductor - uses **indium** tri chloride as an **indium** source.
DC L03 U11
IN KOUKITU, A; MATSUSHIMA, M; MIURA, Y; MOTOKI, K; OKAHISA, T; SEKI, H; SHIMAZU, M; MIURA, S
PA (SUME) SUMITOMO ELECTRIC IND CO; (SUME) SUMITOMO DENKI KOGYO KK
CYC 8
PI EP 801156 A2 19971015 (199746)* EN 14p
R: DE FR GB
JP 09315899 A 19971209 (199808) 10p
TW 332347 A 19980521 (199842)
KR 97068061 A 19971013 (199843)
US 5970314 A 19991019 (199950)
CN 1164759 A 19971112 (200148)
EP 801156 B1 20020904 (200266) EN
R: DE FR GB
DE 69715075 E 20021010 (200274)
ADT EP 801156 A2 EP 1997-302033 19970325; JP 09315899 A JP 1997-87570 19970321; TW 332347 A TW 1997-103683 19970324; KR 97068061 A KR 1997-10253 19970325; US 5970314 A US 1997-823237 19970324; CN 1164759 A CN 1997-104545 19970325; EP 801156 B1 EP 1997-302033 19970325; DE 69715075 E DE 1997-615075 19970325, EP 1997-302033 19970325
FDT DE 69715075 E Based on EP 801156
PRAI JP 1997-87570 19970321; JP 1996-67762 19960325
AB EP 801156 A UPAB: 19971119
A process for vapour-phase epitaxy (VPE) of a compound semiconductor of formula InxGa1-xN (where, 0<x<1) in which InCl3 is used as a source of In. Also claimed is a process as above, where: (a) a conductive substrate, comprising GaAs, GaP, InAS, InP and/or SiC, is placed in a reaction chamber; (b) a first **gas**, comprising InCl3, and a second **gas** comprising NH3 etc., is flown onto the substrate by an inactive carrier **gas**, e.g. N2, He, etc., and a **buffer layer** of InN is grown on the substrate at a first temperature,

whilst the reaction chamber is heated from the outside to maintain this temperature; and (c) a third **gas**, including HCl and an organometallic precursor of **Ga**, is flown with the first and second gases by the carrier **gas**, to grow an epitaxial layer of the compound semiconductor InxGa1-xN on the **buffer layer** by VPE. Further claimed is another process for vapour-phase epitaxy (VPE) of a compound semiconductor of formula InxGa1-xN (where, 0<x<1). Further claimed is a process as above where, helium is used as the carrier **gas**.

USE - Useful for **epitaxial growth** of compound semiconductor devices, especially light-emitting diodes (LEDs) emitting in the blue-green region of the visible spectrum.

ADVANTAGE - Provides a means for VPE of InxGa1-xN with high quality and excellent homogeneity, by improving the mixing of the raw gases, by using a novel source of In, and by choice of the inactive carrier **gas**.

Dwg.2/7

L68 ANSWER 25 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 1997-031449 [03] WPIX
DNN N1997-026698 DNC C1997-009719
TI Semiconductor light emitting element e.g. blue LED mfr. - involves **epitaxial growth** of **indium gallium nitride** relief layer and **indium gallium nitride** light emitting layer sequentially on **indium nitride buffer layer**.
DC L03 U12
IN KOUKITU, A; MATSUBARA, H; MIURA, Y; SEKI, H
PA (SUME) SUMITOMO ELECTRIC IND CO; (SUME) SUMITOMO DENKI KOGYO KK
CYC 3
PI JP 08293473 A 19961105 (199703)* 6p
TW 293951 A 19961221 (199715)
US 5864573 A 19990126 (199911)
ADT JP 08293473 A JP 1995-101351 19950425; TW 293951 A TW 1996-104604 19960418; US 5864573 A US 1996-636563 19960423
PRAI JP 1995-101351 19950425
AB JP 08293473 A UPAB: 19970115
The mfg method includes a gap substrate (1). An InN **buffer layer** (2) is formed on the substrate. An InxGa1-xN relief layer (3) and an InkGa1-kN light emitting layer (4) are formed sequentially on the **buffer layer**.

The value of k lies between zero and one. The value of x in relief layer, gradually reduces from **buffer layer** side (2) light emitting layer side, but remains greater than k.

ADVANTAGE - Improves efficiency. Reduces crystal defect and mfg cost. Prolongs lifetime.

Dwg.1/3

L68 ANSWER 26 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 1996-381590 [38] WPIX
DNN N1996-321791 DNC C1996-120134
TI Growth of **gallium nitride** based semiconductor crystal - where substrate uses specific plane of rare earth Gp IIIB perovskite on which **buffer layer** has been formed.
DC L03 U11
PA (NIHA) JAPAN ENERGY CORP
CYC 1
PI JP 08186329 A 19960716 (199638)* 6p
ADT JP 08186329 A JP 1994-328222 19941228
PRAI JP 1994-328222 19941228
AB JP 08186329 A UPAB: 19960924

In growing a **gallium nitride**-based semiconductor crystal on a substrate, the substrate uses the (101) plane or the (011) plane of a rare earth Gp. 3B perovskite. A **buffer layer** is previously formed on the substrate. The **gallium nitride**-based semiconductor crystal is then grown.

USE - The method grows the **gallium nitride**-based semiconductor crystal. Partic., the method is suitable for applying **epitaxial growth** to a GaN-based semiconductor crystal, including GaN, AlN, InN, and their mixed crystal InxGayAl1-x-yN (x 0; y 0; and x+y at most 1).

ADVANTAGE - Good lattice matching to the GaN-based semiconductor crystal is observed. The (0001) (c plane) of the GaN-based semiconductor crystal is stably grown, via the **buffer layer** on the (101) plane or the (011) plane of the thermally and chemically stable rare earth Gp. 3B perovskite substrate. The method yields the GaN-based semiconductor crystal for a semiconductor material for blue luminescence. Dwg.0/5

L68 ANSWER 27 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 1992-194242 [24] WPIX
CR 1992-202216 [25]
TI Electroluminescent semiconductor device for blue-ultraviolet emission - where P-N junction layers of nitrides are formed by MBE on zinc sulphide-selenide substrate via **buffer layer**.
DC L03 U11 U12
IN KITAGAWA, M; NAKANISHI, K; TOMOMURA, Y
PA (SHAF) SHARP KK
CYC 4
PI GB 2250635 A 19920610 (199224)* 32p
JP 04199752 A 19920720 (199235) 4p
JP 05021847 A 19930129 (199309) 17p
US 5198690 A 19930330 (199315) 28p
US 5237182 A 19930817 (199334) 13p
GB 2250635 B 19940928 (199436)
GB 2250862 B 19941019 (199439)
ADT GB 2250635 A GB 1991-25048 19911126; JP 04199752 A JP 1990-334709 19901129; JP 05021847 A JP 1991-309361 19911125; US 5198690 A US 1991-796684 19911125; US 5237182 A US 1991-798642 19911126; GB 2250635 B GB 1991-25048 19911126; GB 2250862 B GB 1991-25049 19911126
PRAI JP 1990-324346 19901126; JP 1990-331909 19901127; JP 1990-334709 19901129
AB GB 2250635 A UPAB: 19931006
An electroluminescent device of cpd. semiconductor comprises a semiconductor substrate, (1), a **buffer layer** (2) **epitaxially grown** on the substrate and a luminescent layer (4,5) **epitaxially grown** on the **buffer layer** where, a) the substrate is formed from a single crystal of ZnS, ZnSe, or a mixed crystal thereof, and b) the luminescent layer is formed from AlN, InN, GaN or a mixed crystal of at least two nitrides.

USE/ADVANTAGE - The invention provides a solid-state electroluminescent device of cpd. semiconductor which emits in the blue-ultraviolet region. The luminescent epitaxial layer has improved crystallinity and luminescence as a result of the graded **buffer layer**. The method allows a reduced growth temp. for the nitrides which improves doping control and efficiency.
1/9

L68 ANSWER 28 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 1990-280556 [37] WPIX
DNN N1990-234712 DNC C1990-131890
TI Superconducting copper-oxide films - which are grown on cubic

boron nitride and have an intermediate thin film, and **buffer layer** of cubic nitride.

DC L03 U11 U14
PA (DOLL-I) DOLL G L
CYC 1
PI RD 316106 A 19900810 (199037)*
PRAI RD 1990-316106 19900720
AB RD 316106 A UPAB: 19930928
Superconducting copper oxide films may be grown on a Si substrate which has an intermediatem thin film, **buffer layer** of cubic **boron nitride**. The cubic **boron nitride** film provides an inert barrier between the silicon substrate and the overlaying film of superconducting copper oxide.

Single crystal, cubic **boron nitride** thin films have been **epitaxially grown** on a single crystal Si substrate oriented alon along a (001) crystallographic plane using laser ablation deposition methods. The crystallographic lattice constant of the resulting film of cubic **boron nitride** may be varied depending on the laser ablation processing parameters utilised and the orientation of the Si substrate. A cubic **boron nitride** thin film having a lattice constant of approximately 0.38 nm was grown, which was in epitaxial registry with an underlying Si substrate.

The superconducting copper oxide films are such that a perovskite crystal structure having square copper oxide cells have a lattice constant of approximately 0.38 nm. The intermediate **buffer layer** of cubic **boron nitride** should promote the **epitaxial growth** of the superconducting copper oxides because of the cubic **boron nitride**(s reluctance to react chemically with oxygen and the 0.38 nm cubic geometry obtd. when grown on the (100) plane of Si.
0/0

L68 ANSWER 29 OF 46 WPIX (C) 2003 THOMSON DERWENT
AN 1990-280466 [37] WPIX
DNN N1990-216302
TI Base firing frequency RPM spectral power detector for engine - samples engine speed synchronously with crank angle permitting calculation of discrete fourier transform in angle domain.
DC U11 U14
PA (ANON) ANONYMOUS
CYC 1
PI RD 316016 A 19900810 (199037)*
PRAI RD 1990-316016 19900720
AB RD 316016 A UPAB: 19930928
Superconducting copper oxide films may be grown on a Si substrate which has an intermediatem thin film, **buffer layer** of cubic **boron nitride**. The cubic **boron nitride** film provides an inert barrier between the silicon substrate and the overlaying film of superconducting copper oxide.

Single crystal, cubic **boron nitride** thin films have been **epitaxially grown** on a single crystal Si substrate oriented alon along a (001) crystallographic plane using laser ablation deposition methods. The crystallographic lattice constant of the resulting film of cubic **boron nitride** may be varied depending on the laser ablation processing parameters utilised and the orientation of the Si substrate. A cubic **boron nitride** thin film having a lattice constant of approximately 0.38 nm was grown, which was in epitaxial registry with an underlying Si substrate.

The superconducting copper oxide films are such that a perovskite crystal structure having square copper oxide cells have a lattice constant of approximately 0.38 nm. The intermediate **buffer layer**

of cubic **boron nitride** should promote the **epitaxial growth** of the superconducting copper oxides because of the cubic **boron nitride**(s reluctance to react chemically with oxygen and the 0.38 nm cubic geometry obtd. when grown on the (100) plane of Si. @
0/0@

L68 ANSWER 30 OF 46 JAPIO COPYRIGHT 2003 JPO
AN 2002-343728 JAPIO
TI **GALLIUM NITRIDE** CRYSTALLINE SUBSTRATE AND METHOD FOR MANUFACTURING THE SAME
IN USUI AKIRA; SHIBATA MASATOMO; OSHIMA YUICHI
PA NEC CORP
HITACHI CABLE LTD
PI JP 2002343728 A 20021129 Heisei
AI JP 2001-151139 (JP2001151139 Heisei) 20010521
PRAI JP 2001-151139 20010521
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2002
AB PROBLEM TO BE SOLVED: To provide a method for manufacturing a GaN single crystalline substrate which is **epitaxially grown** and has a few defect density.
SOLUTION: A **metal film** deposited on a substrate having a **gallium nitride** single crystal on its surface, the substrate deposited with the **metal film** is heat-treated to form voids in the **gallium nitride** crystal on the substrate, **gallium nitride** is further deposited on the substrate having the voids in the **gallium nitride** crystal to bury the voids, and then a nearly flat single crystalline **gallium nitride** film is grown on the **metal film**.
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L68 ANSWER 31 OF 46 JAPIO COPYRIGHT 2003 JPO
AN 2001-036134 JAPIO
TI SINGLE-POLE LIGHT-EMITTING DEVICE WITH III NITRIDE SEMICONDUCTOR SUPERLATTICE AS BASE
IN WANG WANG NANG; JULIJ GEORGIVICH SHERETAA; JULIJ TOMASOVICH REBAN
PA ARIMA OPTOELECTRONICS CORP
PI JP 2001036134 A 20010209 Heisei
AI JP 2000-179585 (JP2000179585 Heisei) 20000615
PRAI GB 1999-13950 19990615
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To use effective p-n junction for light-emitting between superlattices of a III nitride semiconductor only of n-type by containing a plurality of superlattices, consisting of one out of intrinsic semiconductor, n-type of III nitride semiconductor and an alloy.
SOLUTION: A sapphire substrate 11 is provided, and a **buffer layer** 10 consisting of **aluminum nitride**(AlN) is formed thereon. An n-clad contact layer 5 consisting of n-AlN is laminated thereon. Silicon(Si) is doped to the n-clad contact layer 5. By causing **epitaxially growth** on the n-clad contact layer 5, a shallow sub-band superlattice 3 consisting of Ga0.05Al0.95N/AlN is formed. The sub-band superlattice 3 is constituted by a quantum well 8 consisting of undoped four layers of Ga0.05Al0.95N and a barrier 9 consisting of a four-layer AlN, and a sub-band superlattice 1 is **epitaxially grown**. The su-band superlattice 1 is constituted by a quantum well 7, consisting of undoped three layers of GaN and a barrier 6 which consists of the four-layer AlN.
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L68 ANSWER 32 OF 46 JAPIO COPYRIGHT 2003 JPO

03/21/2003

AN 2001-023903 JAPIO
TI **EPITAXIAL-GROWTH** METHOD OF III-V COMPOUND SEMICONDUCTOR
IN SHIBATA MASATOMO; FURUYA TAKASHI; KIHARA MICHIO
PA HITACHI CABLE LTD
PI JP 2001023903 A 20010126 Heisei
AI JP 1999-193749 (JP11193749 Heisei) 19990707
PRAI JP 1999-193749 19990707
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To prevent the variation of crystal growing conditions and the damage of a flow channel even when byproducts are produced in the flow channel, by forming **metallic layers** made of metal **indium** or metal **gallium**, etc., in the portions of the flow channel whereon the byproducts produced from a raw-material **gas** are deposited easily, and by performing thereafter the growth of a crystal.
SOLUTION: Metal **indium** layers 12 are formed in portions 11 of byproducts being deposited easily thereon when growing a crystal. In a flow channel 2, the metal **indium** layers 12 are formed in a process independent of the formation of the flow channel 2. After integrating the flow channel 2 into an apparatus main body 1, in the atmosphere of an ammonia **gas** fed from a **gas** introducing tube 9, the layers 12 are so heated at a higher temperature than a maximum achievable temperature when growing the crystal epitaxially as to subject the layers 12 previously to heat treatments. On the metal **indium** layers 12, **indium nitrides** 14 are formed. In this way, after forming previously these **metallic layers** 12 made of metal **indium** or metal **gallium**, etc., in the portions of the flow channel 2 made of quartz whereon byproducts are easily deposited, the **epitaxial growth** of the cryatal is performed in the state of these **metallic layers** 12 having been formed.
COPYRIGHT: (C)2001,JPO

L68 ANSWER 33 OF 46 JAPIO COPYRIGHT 2003 JPO
AN 2000-286506 JAPIO
TI **GALLIUM NITRIDE** LIGHT-EMITTING DEVICE
IN YOSHIDA KIYOTERU
PA FURUKAWA ELECTRIC CO LTD:THE
PI JP 2000286506 A 20001013 Heisei
AI JP 1999-91682 (JP11091682 Heisei) 19990331
PRAI JP 1999-91682 19990331
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To obtain the emission of multiple colors from a semiconductor layer that is provided in a single manufacturing process by providing GaN1-yAsy or GaN1-xPx active layer at a V-shaped groove part formed on a substrate.
SOLUTION: A silicon substrate 1 is introduced into a **gas** source molecular beam **epitaxial growth** device, a growth temperature is set to 640°C, a GaN **buffer layer** 2 is grown, then the growth temperature is set to 850°C, a doped GaN layer 3 is grown, then a sample taken out for forming an etching mask 4, and a V-shaped groove row 5 is formed at the Si-doped GaN layer 3 by dry etching. Then, the sample is returned to the growth device, an n-type GaN clad layer 6, an undoped GaN1-yAsy active layer 7, and a P-type GaN clad layer 8 are successively laminated to form semiconductor lamination structure. Therefore, an active layer for performing white-color or arbitrary-color emission can be formed by a simple manufacturing process due to single growth, thus forming a white light-emitting semiconductor device that can be put into a practical industrial application.
COPYRIGHT: (C)2000,JPO

L68 ANSWER 34 OF 46 JAPIO COPYRIGHT 2003 JPO
AN 2000-124500 JAPIO
TI **GALLIUM NITRIDE** SEMICONDUCTOR DEVICE
IN NUNOGAMI SHINYA; YAMAMOTO MASAHIRO
PA TOSHIBA CORP
PI JP 2000124500 A 20000428 Heisei
AI JP 1998-292684 (JP10292684 Heisei) 19981015
PRAI JP 1998-292684 19981015
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To improve the reliability of a **gallium nitride** semiconductor device by preventing the dislocation which occurs at the interface between a substrate and a grown layer from being propagated to the heat of the device, by providing a dislocation propagation preventing layer having projecting sections between the substrate and device and exposing single-crystal faces on the side walls of the projecting sections.
SOLUTION: A washed sapphire substrate 100 is set up in a susceptor in a MOCVD reaction tube, and oxides are removed from the main surface of the substrate 100 on when **gallium nitride** (GaN) layers are to be formed by heating the substrate 100 in a reducing atmosphere. Then a GaN **buffer layer** and a GaN layer 102 are grown on the main surface by making an ammonia **gas** to flow in the reaction tube and, after the substrate 100 is taken out of the reaction tube, stripe-like projecting sections are formed on the surface of the GaN layer 102 through a photolithography process and an etching process. After the projecting sections are formed, a GaN layer 103 is **epitaxially grown** on the projecting section. Since the interface between the GaN layers 102 and 103 is constituted of a single crystal including the side walls of the projecting sections of the GaN layer 102, the growth of the GaN layer 103 in the horizontal direction can be accelerated among the projecting sections, and the total number of defects can be suppressed effectively.
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L68 ANSWER 35 OF 46 JAPIO COPYRIGHT 2003 JPO
AN 1999-284226 JAPIO
TI SEMICONDUCTOR LIGHT EMITTING ELEMENT
IN FUKUYA TOSHIRO; OTSUKA KOJI
PA SANKEN ELECTRIC CO LTD
PI JP 11284226 A 19991015 Heisei
AI JP 1998-100065 (JP10100065 Heisei) 19980327
PRAI JP 1998-100065 19980327
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To inexpensively manufacture a blue light emitting diode using a **gallium nitride** compound in a high-performance state.
SOLUTION: A first **metallic layer** 12 composed of Ti, a second **metallic layer** 13 composed of Pt, a semiconductor area 14 composed of n-type GaN, an active layer 15 composed p-type GaN, and a semiconductor area 16 composed of p-type GaN are successively formed on a substrate 11 composed of n<SP>+</SP>-type silicon containing an impurity at a high concentration by **epitaxial growth**. Then an anode 18 is provided at the center of the upper surface of the p-type semiconductor area 16 and a cathode 19 is provided on the whole lower surface of the low-resistance substrate 11. The **metallic layers** 12 and 13 and semiconductor areas 14 and 16 are grown on the substrate 11 by respectively deciding their crystal orientations.
COPYRIGHT: (C)1999,JPO

L68 ANSWER 36 OF 46 JAPIO COPYRIGHT 2003 JPO
AN 1999-251632 JAPIO
TI MANUFACTURE OF **GALLIUM NITRIDE** SEMICONDUCTOR ELEMENT
IN KATO HISAYOSHI; KOIDE NORIKATSU
PA TOYODA GOSEI CO LTD
PI JP 11251632 A 19990917 Heisei
AI JP 1998-64360 (JP10064360 Heisei) 19980227
PRAI JP 1998-64360 19980227
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To quicken the crosswise growth speed of a semiconductor layer, by forming a foundation layer by ELO(epitaxial lateral overgrowth) where a nitrogen **gas** is used as a carrier. SOLUTION: A monocrystalline-sapphire substrate 2 is subjected to vapor etching, a **buffer layer** 3 made of AlN is formed on the monocrystalline-sapphire substrate 2, a first GaN layer 4 is formed on the **buffer layer** 3, and an SiO<SB>2</SB> film is uniformly formed on the first GaN layer 4 for etching in a stripe shape. A second GaN layer 6 is subjected to **epitaxial growth**. Since the GaN does not grow on a silicon dioxide layer, the GaN layer 6 selectively grows from the surface of the first GaN layer 4 that is not covered with a pattern layer 5. Then, the GaN layer 6 grows crosswise after passing the pattern layer 5 for flattening the upper surface, and the n cladding layer 6 is formed. In the ELO method, a nitrogen **gas** is selected as a carrier **gas**, and the crosswise growth speed of a second GaN semiconductor layer is set to four times faster, thus quickening the growth speed. COPYRIGHT: (C)1999,JPO

L68 ANSWER 37 OF 46 JAPIO COPYRIGHT 2003 JPO
AN 1999-145514 JAPIO
TI **GALLIUM NITRIDE** SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF
IN SUZUKI NOBUHIRO; SUGAWARA HIDETO
PA TOSHIBA CORP
PI JP 11145514 A 19990528 Heisei
AI JP 1997-302918 (JP09302918 Heisei) 19971105
PRAI JP 1997-302918 19971105
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To enable a **gallium nitride** semiconductor thick-film layer of high quality to be grown by a method, wherein a **buffer layer** formed of **indium**-containing **gallium nitride** semiconductor is deposited on a substrate of SiC or Si. SOLUTION: A semiconductor device 10 is formed through a manner where an In<SB>0.1</SB>**Ga**<SB>0.9</SB>N **buffer layer** 12 and a **gallium nitride** semiconductor layer 13 are successively formed in this sequence on a 6H-SiC substrate 11. The **buffer layer** 12 has a function of relaxing stresses caused by a thermal expansion difference between the SiC substrate 11 and the **gallium nitride** semiconductor layer 13. A (0001) substrate is used as the SiC substrate 11, and a **gallium nitride** semiconductor layer possessed of a (0001) plane on its surface is **epitaxially grown** thereon. It is preferable that the **buffer layer** 12 is formed of **indium** - containing **gallium nitride** semiconductor deposited as thick as a monoatomic layer or above, and the **gallium nitride** semiconductor layer 13 corresponds to various device components such as an LED or a laser. The **buffer layer** 12 relaxes stress caused by a thermal expansion coefficient difference to protect a substrate against warpage or cracking. COPYRIGHT: (C)1999,JPO

L68 ANSWER 38 OF 46 JAPIO COPYRIGHT 2003 JPO
AN 1999-135889 JAPIO
TI SUBSTRATE FOR CRYSTAL GROWTH AND LIGHT-EMITTING DEVICE USING THE SAME
IN ISOKAMI MINEO
PA KYOCERA CORP
PI JP 11135889 A 19990521 Heisei
AI JP 1997-299183 (JP09299183 Heisei) 19971030
PRAI JP 1997-299183 19971030
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To grow a GaN thin film of good quality, having extremely few defects by the use of a sapphire as a base substrate, and forming on the surface thereof a compound layer having a misfit ratio for **gallium nitride** smaller than that of sapphire.
SOLUTION: A sapphire substrate having a C face as a main face is used, ions of at least one element selected form a group consisting of **Al**, Si, Mg, Zn, Ti, **Ga**, Y, O, N, and C are implanted into the substrate as an ion composing a material, having a small misfit ratio to form a compound layer, and the layer is heat-treated at a temperature above 1,000°C to make a substrate for **epitaxial growth**. A semiconductor laser diode comprises a compound layer formed by ion-implantation on the main face 1a of a substrata 1, a **buffer layer** 2 comprising an amorphous **gallium nitride** or an AlN(**aluminum nitride**) layer formed on the main face 1a, and a multilayered layer 3 of a semiconductor formed on the **buffer layer** 2.
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L68 ANSWER 39 OF 46 JAPIO COPYRIGHT 2003 JPO
AN 1999-097638 JAPIO
TI SEMICONDUCTOR MEMORY AND MANUFACTURE OF THE SAME
IN KAWAKUBO TAKASHI; FUKUSHIMA SHIN
PA TOSHIBA CORP
PI JP 11097638 A 19990409 Heisei
AI JP 1997-251543 (JP09251543 Heisei) 19970917
PRAI JP 1997-251543 19970917
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To enable higher integration with an easy manufacturing method by providing a transistor connected to a capacitor having first and second electrodes formed inside a groove on a specified surface of silicon through **epitaxial growth**.
SOLUTION: Using a first Si substrate 1, a trench surrounded by (100) orientation for embedding a capacitor is formed by an etching method. Next, (Ti, **Al**) **N** is **epitaxially grown** as a barrier **metal layer** 2.
Subsequently, as a first electrode 3, SrRuO<SB>3</SB>(SRO) is **epitaxially grown** conformally. As a second electrode 5, SRO is eqitaxially grown and embedded in the trench. Next, a groove is formed in a silicon layer 7 of a SOI substrate, and an insulating film is embedded in the groove, thus forming a trench-isolated type element isolation film (STI) 9. Using etching conditions based on this STI 9, a source/drain impurity layer 13, word lines 15a ad 15b and the like are formed, thus producing a transistor.
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L68 ANSWER 40 OF 46 JAPIO COPYRIGHT 2003 JPO
AN 1998-291894 JAPIO
TI SUBSTRATE FOR CRYSTAL GROWTH AND LIGHT EMITTING DEVICE
IN SUDA NOBORU; ISOKAMI MINEO
PA KYOCERA CORP
PI JP 10291894 A 19981104 Heisei

AI JP 1997-104916 (JP09104916 Heisei) 19970422
PRAI JP 1997-104916 19970422
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998
AB PROBLEM TO BE SOLVED: To obtain a substrate for crystal growth which can be produced at a low melting point, which enables preferable vapor phase growth such as **epitaxial growth** of **gallium nitride**, and which is inexpensive and excellent, and to obtain a light-emitting device using this substrate. by constituting the substrate of an olivine-type single crystal as the main component.
SOLUTION: This substrate for crystal growth essentially consists of an olivine-type single crystal and is used for vapor phase growth of a single crystal essentially comprising **gallium nitride**.
Moreover, an amorphous or crystalline **buffer layer** may be formed between the substrate for crystal growth and a single crystal layer essentially comprising **gallium nitride**. This olivine-type single crystal is a solid soln. having the chemical compsn. containing one or more of Mg<SB>2</SB>SiO<SB>4</SB>, Mn<SB>2</SB>SiO<SB>4</SB> and Co<SB>2</SB>SiO<SB>4</SB>. The light-emitting device LD has, for example, a **buffer layer** 2 comprising an amorphous AlN layer on the principal plane 11 of the substrate 1, and has a laser element comprising multilayered single crystal layers 31 to 35 essentially comprising **gallium nitride** on the **buffer layer** 2.
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L68 ANSWER 41 OF 46 JAPIO COPYRIGHT 2003 JPO
AN 1998-242520 JAPIO
TI **GALLIUM NITRIDE** COMPOUND SEMICONDUCTOR ELEMENT AND ITS MANUFACTURE
IN GOTO JUN; MINAGAWA SHIGEKAZU; KAWADA MASAHIKO; AKAMATSU SHOICHI
PA HITACHI LTD
PI JP 10242520 A 19980911 Heisei
AI JP 1997-45231 (JP09045231 Heisei) 19970228
PRAI JP 1997-45231 19970228
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998
AB PROBLEM TO BE SOLVED: To obtain an excellent ohmic junction between an electrode structure and a p-type layer, by constituting the electrode structure of a multilayered film which is composed of an alloy containing Ni and Mg or in which Ni and Mg are laminated upon another as part of the electrode material for a **gallium nitride** compound semiconductor element.
SOLUTION: A sapphire substrate 1, an amorphous GaN **buffer layer** 2, and a p-type Mg-doped GaN layer 3 are provided. The layers 2 and 3 are successively grown on the substrate crystal 1 by using a metal organic vapor phase **epitaxial growth** device.
For example, trimethyl **gallium**(TMGa) and cyclopentadienyl magnesium(Cp<SB>2</SB>Mg) are used as raw materials. Ni and Mg are vapor-deposited by the heater vapor deposition method, and Ti and Pt are vapor deposited by the electron beam vapor deposition method. Finally, Au is vapor deposited by the lift off method. After the Au is vapor-deposited, an At/Pt/Ti/Mg/Ni electrode 4 is formed by the lift off method.
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L68 ANSWER 42 OF 46 JAPIO COPYRIGHT 2003 JPO
AN 1998-079530 JAPIO
TI LIGHT-EMITTING DIODE FOR **GALLIUM NITRIDE** COMPOUND SEMICONDUCTOR
IN NITTA KOICHI
PA TOSHIBA CORP
PI JP 10079530 A 19980324 Heisei

AI JP 1997-181392 (JP09181392 Heisei) 19970707
PRAI JP 1996-178032 19960708
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998
AB PROBLEM TO BE SOLVED: To enable a light-emitting diode to be lessened in chip area and enhanced in degree of integration by a method, wherein an anode electrode and a cathode electrode are provided to the front side and rear side of a conductive substrate respectively.
SOLUTION: An n-type **gallium nitride** compound semiconductor **buffer layer** 5 is grown on the one primary surface of a conductive substrate 3. Then, an n-type **gallium nitride** compound semiconductor layer 7, a **gallium nitride** compound semiconductor layer 9, and a p-type **gallium nitride** compound semiconductor layer 11 are successively laminated thereon through an organometallic vapor growth method, a molecular beam **epitaxy growth** method or the like for the formation of a **gallium nitride** compound semiconductor light-emitting device 1. A current injection anode electrode 13 is formed on the p-type **gallium nitride** compound semiconductor layer 11, and a cathode electrode 15 is formed on the other primary surfaces of the conductive substrate 3. Therefore, two bonding wires are not required to be bonded on the same plane. By this setup, bonding wires can be bonded without taking bonding accuracy into consideration, and a semiconductor light-emitting diode of this constitution can be lessened in chip area and enhanced in degree of integration.

L68 ANSWER 43 OF 46 JAPIO
AN 1998-075018 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR AND SEMICONDUCTOR LIGHT-EMITTING DEVICE
IN ISHIBASHI AKIHIKO; BAN YUZABURO; HARA YOSHIHIRO; KAMIMURA NOBUYUKI; KUME MASAHIRO
PA MATSUSHITA ELECTRIC IND CO LTD
PI JP 10075018 A 19980317 Heisei
AI JP 1997-143868 (JP09143868 Heisei) 19970602
PRAI JP 1996-153953 19960614
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998
AB PROBLEM TO BE SOLVED: To provide a **gallium nitride** semiconductor which has high quality and has good electrical and chemical characteristics.
SOLUTION: An SiC semiconductor substrate 11 is dipped in a buffered hydrofluoric acid for 10 minutes, and an oxide film on the surface of the semiconductor substrate 11 is removed by etching. Using metal organic vapor phase **epitaxial growth** technology (MOVPE method), TMA(trimethylaluminum), NH<SB>3</SB>, and hydrogen for carrier are supplied onto the semiconductor substrate 11 at 1090°C at the rate of 10μmol, 2.5L, and 2L per minute respectively to grow a **buffer layer** 12 which is made of single crystal AIN and is 15nm in thickness kon a principal plate of the semiconductor substrate 11. Nextly, the temperature is decreased to 800°C and TMA, TMG(trimethylgallium), TMI(trimethylindium), and NH<SB>3</SB> are supplied at the rate of 0.2μmol, 2μmol, 20μmol, and 5L per minute respectively to grow an AlGaInN single crystal layer 13 on the **buffer layer** 12.

L68 ANSWER 44 OF 46 JAPIO
AN 1998-041232 JAPIO
TI COMPOUND SEMICONDUCTOR ELEMENT
IN UDAGAWA TAKASHI
PA SHOWA DENKO KK

PI JP 10041232 A 19980213 Heisei
AI JP 1996-197598 (JP08197598 Heisei) 19960726
PRAI JP 1996-197598 19960726
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998
AB PROBLEM TO BE SOLVED: To sufficiently cover the surface of a deposited layer with a low- temperature **buffer layer** by forming a compound semiconductor **buffer layer** comprising a single-crystal layer and a spheric single crystal having a specific particle size on the surface of a substrate crystal and further depositing a **gallium nitride**-based compound semiconductor layer.
SOLUTION: A light emitting element comprises a laminate composed of layers 112-126 formed on, for example, a sapphire substrate 101 having, for example, (0001)-face (C-face) as a preform. The layer 122 is a GaN low-temperature **buffer layer** which mainly comprises a nearly spheric body composed a single-crystal layer having a thickness (t) in an as-grown state and a spheric body composed mainly of a single crystal having a diameter of 0.1t to 5.0t. The layer 122 is formed by using, for example, the well known organo- metallic thermal decomposition vapor growth method or a vapor phase **epitaxial growth** method, such as the VPE growth method, etc. On the layer 122, the **gallium nitride** layers 123-126 are growth at high temperatures.

L68 ANSWER 45 OF 46 JAPIO COPYRIGHT 2003 JPO
AN 1996-083928 JAPIO
TI SEMICONDUCTOR LIGHT EMITTING ELEMENT AND MANUFACTURE THEREOF
IN TAJIRI HIROSHI
PA ROHM CO LTD
PI JP 08083928 A 19960326 Heisei
AI JP 1994-218551 (JP06218551 Heisei) 19940913
PRAI JP 1994-218551 19940913
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1996
AB PURPOSE: To improve the light emitting efficiency with a low cost by laminating a **gallium nitride** compound semiconductor layer having at least an n-type layer and a p-type layer on a substrate made of a silicon oxide substrate.
CONSTITUTION: The one surface of a silicon oxide plate is mirror polished as a substrate 1, and an n-type GaN film is formed thereon by an MOCVD method. When the film forming temperature is low temperature of about 400-700°C, the GaN is formed in a film in a polycrystalline state to become a low temperature **buffer layer** 2. Thereafter, when it is **epitaxially grown** at a high temperature of 900-1200°C, a high temperature **buffer layer** 3 made of GaN single crystalline layer is formed. Further, an n-type clad layer 4, an active layer 5, a P-type clad layer 6 and a cap layer 7 are grown, and a **gallium nitride** compound semiconductor is laminated. Thus, since it can be formed on a low-cost silicon oxide substrate, a lower-cost blue semiconductor light emitting element than a sapphire can be obtained.

L68 ANSWER 46 OF 46 JAPIO COPYRIGHT 2003 JPO
AN 1981-134780 JAPIO
TI MANUFACTURE OF BEAM LEAD TYPE SCHOTTKY DIODE
IN HARADA YASOO
PA SANYO ELECTRIC CO LTD
PI JP 56134780 A 19811021 Showa
AI JP 1980-39204 (JP55039204 Showa) 19800326
PRAI JP 1980-39204 19800326
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1981

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AB PURPOSE: To simplify the process by performing etching through the window in an **Al** layer on the substrate surface, providing a connecting hole for the second beam lead, using the **Al** as a mask in filling an electrode metal, and decreasing the mask alignment.
CONSTITUTION: An n<SP>++</SP> layer 11 and an n layer 12 are **epitaxially grown in n**<SP>+</SP>
GaAs 10. Al14 is evaporated, a resist mask 15 is provided, and etching is performed. The connecting hole 17 reaching a layer 11 is made. Then, an Au-Ge-Ni film 18 is evaporated, the resist 15 is removed, heat treating is performed, and a **metal film** 18 and the n<SP>++</SP>
layer 11 are ohmic-contacted. Then electric plating is performed only on the film 18, and the hole 17 is filled. At this time, the oxidizing property of the surface of **Al** 14 is strong as acts as a mask. A resist mask 15' is provided again, a window 20 is opened in Al14, a Ti-Mo-Au film 21 is evaporated, the resist is removed, polyimide resin film 22 and an Au-Ti film 23 are laminated, and the first and second Au beam leads 24 and 25 are attached.